DEVELOPMENT OF NOVEL, HIGH-SPEED GAAS AND INGAAS PHOTODETECTORS FOR OPTICAL COMPUTING AND COMMUNICATIONS

By

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Abstract of Dissertation Presented to the Graduate School
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Development of low-noise, high-speed photodetectors (up to 50 GHz) as well as their optimum package for optical computing and communications are presented. For the low-noise high-speed photodetectors, planar GaAs and $In_{.53}Ga_{.47}As$ Schottky barrier photodiodes have been designed, fabricated, and characterized. Furthermore, impedance matching networks with minimum parasitics have been developed to deliver the maximum power of a high-speed photodetector to the external load without any significant attenuation and distortion.

For the detection of short wavelength optical signals, a high-speed, high-sensitivity planar $GaAs/Al_{0.3}Ga_{0.7}As$ heterostructure Schottky barrier photodiode has been developed. Incorporation of a planar geometry, an $Al_{0.3}Ga_{0.7}As$ buffer layer, and a Si_3N_4 passivation layer has significantly improved the detection performances, i.e., response-speed and sensitivity. The external quantum efficiency and responsivity are $60 \sim 77$ % and $0.47 \sim 0.6$ A/W, respectively. The sampling/correlation measurements have shown that the risetime of the photodiode is 8.5 ps, which is compatible to the 3-dB cutoff frequency of 50 GHz.

For long wavelength use, a high-speed $In_{.53}Ga_{.47}As$ planar back-to-back Schottky barrier photodiode has been designed, fabricated, and characterized. The external quantum efficiency and responsivity of the polyimide coated photodiode are $48 \sim 69$ % and $0.49 \sim 0.56$ A/W, respectively. The 3-dB cutoff frequency of 2.7 GHz has been determined from the RC time constant of the equivalent circuits.

The effective Schottky barrier height of n-$In_{.53}Ga_{.47}As$ has been enhanced, for the first time, by using a novel graded-superlattice of $In_{.53}Ga_{.47}As/In_{.52}Al_{.48}As$ grown by molecular beam epitaxy (MBE). Overall effective Schottky barrier height of 0.71 and 0.60 eV for Au and Cr, respectively, have been achieved. In addition, excellent current-voltage and capacitance-voltage characteristics have been obtained. This novel graded-superlattice can eliminate a pile-up of carriers at the heterointerface, and hence can be used for high-speed electronic and optoelectronic device applications.

In order to minimize the packaging parasitics of a high-speed photodetector, impedance matching networks have been developed by employing microstrip transmission line and coplanar waveguide. The design procedures for the impedance matching networks consist of the graphical approximation, the computer aided circuit synthesis and optimization, and the evaluation. In addition, based on the characteristics of the microstrip line, the planar lumped elements such as inductor, capacitor, resistor, and junction discontinuity have been analyzed and synthesized.

CHAPTER ONE
INTRODUCTION

Applications for high-speed photodetectors include optical communication, microwave generation, microwave transmission through optical fibers, microwave delay lines, optical time domain reflectometry, dispersion measurement of optical fibers and microwave transmission lines, and generation of short electrical pulses. Recently, with the introduction of femtosecond laser pulse technology and lightwave modulation in the several tens of gigahertz frequency range, development of high-speed broad bandwidth photodetectors is necessary for the giga-bit rate lightwave communications as well as for the integrated optoelectronic applications [1-3]. To meet this purpose, various types of photodetectors have been developed, for examples, p-i-n [4-12], Schottky barrier [13-18], photoconductor [19-25], and avalanche photodiode [26-31], and summarized in Table 1.1.

The main objectives of this dissertation are the development of high-speed photodetectors (up to 50 GHz) and the optimum package for optical computing and communications. The design requirements of photodetectors and package are summarized in Table 1.2. Of the principal compound semiconductors for lightwave applications, as is shown in Fig.1.1, GaAs and $In_{.53}Ga_{.47}As$ lattice-matched to InP substrate are the most suitable materials for the detection of optical signals of interest. In addition, a planar structure of Schottky barrier has advantages such as simplicity of fabrication and integration. Therefore, for the low-noise, high-speed photodetectors, n-type GaAs and p-type $In_{.53}Ga_{.47}As$ planar Schottky barrier photodiodes have been designed, fabricated, and characterized. In order to minimize the packaging parasitics, which may attenuate or distort both electrical and optical signals if not properly designed, it is necessary to optimize the package by employing microstrip transmission line or coplanar waveguide.

Table 1.1 Overview of III-V semiconductor high-speed photodetectors.

Type	Structure	Characteristics	Institute	Reference
p-i-n	GaAs Planar	$f_c = 20$ GHz	Lincoln Lab.	5
	GaAs/AlGaAs Planar	$f_c = 2.5 \sim 20$ GHz	Ortel Corp.	4
	InGaAs Planar	$t_{rise} = 60$ ps	Bell Lab.	12
	InGaAs/InP Planar	$t_{rise} = 35$ ps	TRW	11
Schottky Barrier	GaAs Mesa	$f_c = 18$ GHz	Hughes	15
	GaAs Planar	$f_c = 100$ GHz	Hewlett Packard	14
	InGaAs Mesa	$f_c = 13.5$ GHz	Univ. of Florida	18
	InGaAs Planar	$t_{rise} = 15$ ps	Aachen Univ.	17
Photo-Conductor	GaAs	$f_c = 4.5$ GHz	Hughes	19
	GaAs/AlGaAs	$f_c = 15$ GHz	Hughes	20
	InGaAs	$t_{rise} = 20$ ps	Aachen Univ.	23
	InGaAs	$f_c = 130$ MHz	Bell Lab.	24
APD	InGaAs Mesa	$t_{rise} = 250$ ps	Thomson/CSF	26
	GaAs Superlattice	$\alpha/\beta = 8$	Bell Lab.	29
	InGaAs SAGM	FWHM=100 ps	Bell Lab.	30

Table 1.2 Design requirements of low-noise high-speed photodetectors.

Wavelength	$0.8 \sim 1.7\ \mu$m
Operating Frequency	~ 50 GHz
Quantum Efficiency	$\sim$50 %
Responsivity	~ 0.5 A/W
Dark Current	≤ 1.0 nA
Structure	Planar Schottky Barrier
Input Impedance	50 Ω

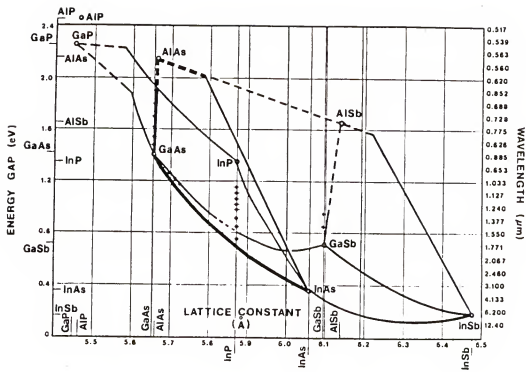


Figure 1.1 Energy bandgap (wavelength) and lattice constant for several III-V compound semiconductors.

In chapter two, general photodetector parameters related to the design requirements, such as spectral response, response speed, dark current, d.c. parameters, and noise equivalent power, are theoretically analyzed. Device packaging and response speed measurements are also described. In chapter three, surface passivation and antireflection coating for GaAs and InGaAs Schottky barrier photodiodes with various dielectric films such as SiO_2, Si_3N_4, and polyimde, are systematically investigated. In chapter four and five, low-noise high-speed planar GaAs/$Al_{0.3}Ga_{0.7}As$ and $In_{.53}Ga_{.47}As$ Schottky barrier photodiodes are designed, fabricated, and characterized. In chapter six, enhancement of the effective Schottky barrier height on n-$In_{.53}Ga_{.47}As$ using a novel graded-superlattice is described. In chapter seven, analysis and synthesis of microstrip transmission lines are discussed based on both quasi-static TEM model and dispersion model. In addition, impedance-matched optimum packaging of a high-speed photodetector is described by employing the lumped and distributed elements of microstrip line. Chapter eight presents summary and conclusions, as well as recommendations for the further study on the monolithically integrated high-speed photoreceiver modules.

CHAPTER TWO
THEORETICAL ANALYSIS OF PHOTODETECTOR PARAMETERS

The primary design requirements for a high-speed photodetector include (1) high quantum efficiency, (2) low dark current, (3) low capacitance and resistance, and (4) low excess noise (especially for avalanche photodiode). These detector requirements are tied to the particular material requirements [32]:

1. A direct energy bandgap smaller than the photon energy to be detected.
2. High-quality and low-defect density epilayers lattice-matched to the substrate.
3. A dopant density to optimize the depletion layer width, which is a trade-off between speed and quantum efficiency.

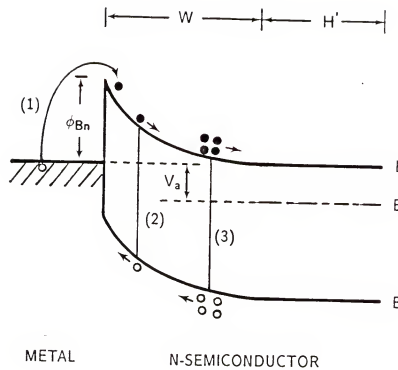
2.1. Spectral Response

The schematic band diagram and the detection modes of the Schottky barrier photodiode are shown in Fig.2.1. Considering two main photocurrents coming from the depletion region and the quasi-neutral base region, the external quantum efficiency, η, of the Schottky barrier photodiode can be expressed by [33]

$$\eta(\lambda) = [1 - R(\lambda)]\left[1 - e^{-\alpha W}\left\{1 - \frac{\alpha L_{p,n}}{\alpha^2 L_{p,n}^2 - 1}\left[\alpha L_{p,n} - \frac{\cosh(H'/L_{p,n}) - e^{-\alpha H'}}{\sinh(H'/L_{p,n})}\right]\right\}\right] \quad (2.1)$$

where Φ is the incident photon flux density, R the reflection loss of the metal film, α the absorption coefficient, W the depletion layer width, and H (= H′ + W) the thickness of the epilayer.

As shown in the above equation, the quantum efficiency of a transparent Schottky barrier photodiode is determined mainly by the reflection loss at the air-metal interface and



(1) $q\phi_{Bn} < h\nu < E_g$, $V_a < V_B$

(2) $h\nu > E_g$, $V_a < V_B$

(3) $h\nu > E_g$, $V_a \simeq V_B$

Figure 2.1 Schematic band diagram and detection modes of the Schottky barrier photodiode. (V_a:applied voltage, V_B:breakdown voltage, and ϕ_{Bn}:Schottky barrier height)

the width of the depletion (absorption) layer. To reduce the reflection loss, an anti-reflection (AR) coating of Ta_2O_5, SiO_2, Si_3N_4, or polyimide films of thickness equal to the quarter wavelength of the incident photon is usually used. The thickness of a single AR coating film is given by [34]

$$d_1 = \frac{\lambda_o}{4\pi n_1} \tan^{-1}\left(\frac{2n_1 k_s}{n_1^2 - n_s^2 - k_s^2}\right) \tag{2.2}$$

where λ_o is the wavelength of the incident photon, n_1 is the refractive index of the dielectric film, and n_s and k_s are the complex refractive indices of semiconductor. The minimum reflection loss with a quarter wavelength AR coating can be expressed by

$$R_{min} = \left(\frac{n_1^2 - n_{air} n_s}{n_1^2 + n_{air} n_s}\right)^2 \tag{2.3}$$

where n_{air} is the refractive index of air.

2.2. Response Speed

The response speed of a photodetector can be determined primarily by three parameters; the transit time (t_{tr}) across the depletion region, the diffusion time (t_{diff}) in the quasi-neutral region, and the RC time constant (t_{RC}) required to discharge the junction capacitance through a combination of internal and external resistances. The total risetime of a photodiode, which is defined as the response time from 10 to 90 % of a pulse height, can be expressed by

$$t_{tot} = (t_{tr}^2 + t_{diff}^2 + t_{RC}^2)^{1/2} = \frac{0.35}{f_c} \tag{2.4}$$

where f_c is the bandwidth (3-dB cutoff frequency) of a photodiode.

When carriers are generated in the depletion region, they should be collected by traversing across the depletion region. The carrier drift (transit) time across the depletion region is given by [35]

$$t_{tr} = \frac{W}{2.8 v_s} \tag{2.5}$$

where v_s is the saturation drift velocity of the carriers, and W is the depletion layer width. This expression is strictly true only for the injected carriers through the junction of constant

electric field, but it remains a reasonable approximation for the photo-generated carriers in that region. It should be noted that the depletion layer width is a trade-off between the response speed and the quantum efficiency.

The carriers generated in the quasi-neutral region will diffuse to the drift region. This carrier diffusion will result in a time delay of the carriers reaching the drift region. The diffusion time is given by [35]

$$t_{diff} = \frac{W_{p,n}^2}{2.43 D_{n,p}} \tag{2.6}$$

where $W_{p,n}$ is the thickness of the quasi-neutral epilayer and $D_{p,n}$ is the diffusion constant.

A time constant of lumped circuit elements for a photodiode also limits its response speed through the junction capacitance (C_j), the series resistance (R_s), and the load resistance (R_L). The shunt resistance (R_i) connected in parallel to the junction capacitance is generally very high, and is considered to be open. Therefore, the RC time constant is given by

$$t_{RC} = (R_s + R_L)C_j \tag{2.7}$$

For high speed operation, the series resistance and the junction capacitance should be small and the load resistance is typically fixed to 50 Ω.

2.3. Dark Current

The dark current of a photodetector should be minimized for the purpose of improving the minimum detectable power level of the incident light. For the Schottky barrier photodiode, the dark current consists of the thermionic-emission current over the Schottky barrier, the generation-recombination current via traps in the depletion region, the tunneling current across the bandgap, and the surface leakage current or interface current due to traps at the metal-semiconductor interface. Since the tunneling current can be neglected for low doped semiconductors, and surface leakage current can also be eliminated by careful processing and proper passivation, the thermionic-emission current over the Schottky barrier and the

generation-recombination current in the depletion region are the main components of the dark current for the Schottky barrier photodiode. In fact, the generation-recombination current can also be eliminated in a high quality Schottky barrier photodiode.

The dark current of a Schottky barrier diode under the forward bias condition is determined mainly by thermionic-emission of majority carriers from the semiconductor into the metal, and can be expressed by [36]

$$J_{th} = A^* T^2 \exp(\frac{-q\phi'_{Bn}}{kT})[\exp(\frac{qV}{nkT}) - 1] \tag{2.8}$$

where A^* is the Richardson's constant, ϕ'_{Bn} the effective barrier height, n the ideality factor.

In thermal equilibrium, the generation rate of electron-hole pairs in the depletion region is balanced by the recombination rate. In the presence of applied bias voltage, however, there will be a net generation or recombination current depending on the polarity of the bias. The generation-recombination current through the midgap traps in the depletion region, which is dominant at low voltage, is given by [37]

$$J_{gr} = \frac{qn_i W}{\tau_{eff}}[\exp(\frac{qV}{2kT}) - 1] \tag{2.9}$$

where $\tau_{eff} = (\tau_n \tau_p)^{1/2}$ is the effective carrier lifetime in the depletion region.

Tunneling current either via band-to-band or via deep-level traps dominates the dark current at high voltage, resulting in the soft breakdown characteristics. For heavily doped semiconductors, the field emission becomes more important than the thermionic emission, and the exponential dependence of the current changes from qV/kT to qV/E_∞ [38].

$$J = J_s \exp\left(\frac{qV}{E_\infty \coth(E_\infty/kT)}\right) \tag{2.10}$$

$$E_\infty = \frac{qh}{4\pi}\sqrt{N_D/m^*\epsilon_s} \tag{2.11}$$

where h is the Plank's constant, and m^* and ϵ_s are the effective mass of electron and the permitivity of semiconductors, respectively. E_∞ is a very useful parameter in predicting the relative importance of the thermionic emission and the tunneling. For $E_\infty/kT \ll 1$, the

thermionic emission process is dominant and the contact behaves as the Schottky barrier. For $E_{\infty}/kT \gg 1$, the field emission process is dominant and the contact exhibits the ohmic characteristics. For $E_{\infty}/kT \simeq 1$, a mixed mode of transport occurs.

2.4. D.C. Parameters: Capacitance, Resistance, and Inductance

The total capacitance of a packaged Schottky barrier photodiode is given by

$$C_{Tot} = C_j + C_o + C_p \tag{2.12}$$

where C_j is the metal-semiconductor junction capacitance, C_o is the overlay capacitance across the passivation layer, and C_p is the package parasitic capacitance. For high-speed applications, the overlay and package parasitic capacitances should be minimized.

The junction capcitance is simply given by the one-sided abrupt junction analysis, and is expressed by [39]

$$C_j = A\sqrt{\frac{q\epsilon_o\epsilon_s N_D}{2(V_{bi} - V - kT/q)}} \tag{2.13}$$

where N_D is the dopant density and V_{bi} is the built-in potential.

The capacitance due to the metal contact overlaying the passivating dielectric layer in the Schottky barrier diode can be approximated by

$$C_o = A\frac{\epsilon_o\epsilon_s}{W} \tag{2.14}$$

where W is the thickness of the dielectric layer and A is the area of the dielectric layer.

The series resistance is composed of the lead resistance, the spreading resistance of the base material, and the sheet resistance of the epilayer and the substrate. The series resistance is due mainly to the sheet resistance of the semiconductor substrate and the undepleted epilayer. This resistance is distributed, depending on the contact geometry, and is frequency dependent. The series resistance of the epilayer is given by

$$R_s = \frac{W}{qA\mu_{p,n}N_{A,D}} \tag{2.15}$$

where W thickness of the epilayer, $\mu_{p,n}$ mobility of carriers, and $N_{A,D}$ the dopant density.

The intrinsic response speed of a photodiode is usually degraded by the external circuit elements, such as junction and parasitic capacitances, series and load resistances, and inductances. The inductance is due primarily to the bonding wire. If a round wire is used, the inductance L_b (nH) can be estimated by [40]

$$L_b = 5.08 \times 10^{-3} L \left[\ln\left(\frac{L}{d}\right) + 0.386 \right] \tag{2.16}$$

where d (mil) is the diameter of the bond wire. If a metal ribbon of width W, thickness t, and length L is used, the inductance due to the metal ribbon can be expressed by [40]

$$L_b = 5.08 \times 10^{-3} L \left[\ln\left(\frac{L}{W+t}\right) + 1.19 + 0.022\frac{W+t}{L} \right] \tag{2.17}$$

2.5. Noise Equivalent Power

The minimum detectable optical power of an incident light is limited by the noise performance of a photodiode. The noise of a photodiode under reverse bias condition is a combination of shot noise and thermal noise (Johnson noise). The shot noise is due to the background illumination (I_B), the photogenerated current (I_p), and the reverse-bias dark current (I_D), and can be written as

$$\overline{i_s^2} = 2q(I_p + I_B + I_D)\Delta f \tag{2.18}$$

where Δf is the bandwidth. The thermal noise arises from a random motion of the carriers within any resistive materials including semiconductors, and is given by

$$\overline{i_T^2} = \frac{4kT\Delta f}{R_{eff}} \tag{2.19}$$

where $1/R_{eff}$ is the effective resistance of the photodiode.

An intensity modulated optical signal can be expressed as

$$P(\omega) = P_{opt}(1 + me^{j\omega t}) \tag{2.20}$$

where P_{opt} is the average optical signal power, m the modulation index, and ω the modulation frequency. Then, the rms photocurrent due to the rms optical signal can be given by

$$i_p = \frac{q\eta m P_{opt}}{\sqrt{2}h\nu} \tag{2.21}$$

For a 100% modulated siganl with average power P_{opt}, the signal-to-noise ratio (SNR) is given by

$$SNR = \frac{i_p^2 R_{eff}}{(\overline{i_s^2} + \overline{i_T^2})R_{eff}} \tag{2.22}$$

$$= \frac{(1/2)(q\eta P_{opt}/h\nu)^2}{2q(I_p + I_B + I_D)\Delta f + 4kT\Delta f/R_{eff}} \tag{2.23}$$

Another related figure of merit for photodetectors is the noise-equivalent power (NEP) which defines the incident rms optical power required to produce a SNR of one in a 1-Hz bandwidth. The NEP can be obtained from the above expression by setting SNR=1 and $\Delta f = 1$ [39].

$$NEP = \frac{h\nu}{\eta}\sqrt{2\left(\frac{I_B + I_D}{q} + \frac{2kT}{R_{eff}}\right)} \tag{2.24}$$

To improve the sensitivity of the photodiode, both η and R_{eff} should be maximized while I_B and I_D should be minimized.

2.6. Packaging

A photodetector should be packaged to protect from mechanical or other possible damages and to allow its incorporation into electrical and optical circuits. However, if not properly designed, packaging introduces additional parasitic effects which may attenuate or distort both electrical and optical signals. In packaging a high-speed photodetector for optical fiber communications, there are two kinds of packages to be considered: One is the optical link between a optical fiber and a photodiode, which should ensure the maximum quantum efficiency and the minimum background illumination. The other is the electrical link between a photodiode and a test fixture by using transmission lines. In the latter

case, both microstrip transmission line and coplanar waveguide are commonly used for the high-speed operation.

Since the lumped/distributed passive elements can be fabricated on the same substrate, microstrip transmission lines have been extensively used for microwave and millimeter-wave integrated circuits for frequencies ranging from a few GHz to several tens of GHz. At higher frequencies, particularly into the millimeter wavelength range, losses increase greatly and the higher-order modes become a considerable problem [41]. The frequency limit for the use of microstrip transmission line is around 100 GHz. The detailed analysis and synthesis of the microstrip line and the impedance matching networks for the optimum packaging of a high-speed photodetector will be discussed in chapter seven.

2.7. Response Speed Measurements

2.7.1. Impulse Response

This method [42,43] requires an optical source generating ultrashort pulses shorter than the impulse response of the photodetector to be measured. For broadband characterization, either a synchronously pumped mode-locked dye laser or a diode laser driven by a comb generator (or a step-recovery diode) is necessary. The schematic diagram for the impulse response measurement is shown in Fig.2.2. The impulse response is measured either by a sampling scope in the time domain or by a microwave spectrum analyzer in the frequency domain.

Note that the measured response is a convolution of the true photodetector impulse response and the measurement system response including the sampling gate width, the laser pulse width, the pulse broadening due to transmission lines and connectors. Since most of these are not known accurately, it is difficult to estimate the true impulse response of the photodetector by deconvolution. A more accurate estimation can be obtained by an electrical correlation measurement using two identical photodetectors.

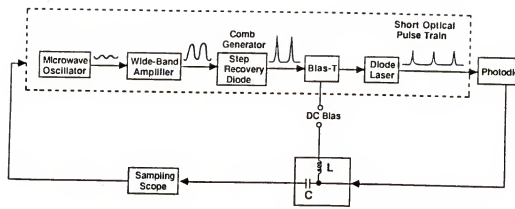


Figure 2.2 Schematic diagram for the impulse response measurement.

2.7.2. Sampling/Correlation

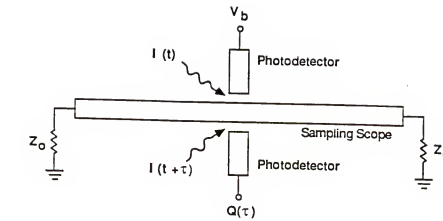
A standard technique for measuring the duration of a picosecond optical pulse is to make a nonlinear optical auto-correlation of two identical optical pulses by delaying one with respect to the other and by mixing them in a second harmonic generating crystal [44,45]. This method requires two photodetectors, each of which is activated by a picosecond optical pulse. The output signal from the first photodetector is used to bias the second one. The photodetectors are not necessarily identical, in which case the measurement is referred to a cross-correlation.

The photodetectors are connected in order that the device under test launches a waveform onto a transmission line by an incidenting short optical pulse and the second photodetector acts as a sampling gate on the transmission line probed by the same optical pulse with a variable time delay. The schematic diagrams are shown in Fig.2.3. The variable delay can be introduced by varying the relative timing of the optical pulses absorbed at each photodetector. The experimentally measured quantity is the total charge sampled at the output of the second photodetector as a function of the relative delay between the two optical pulses.

The measurement correlates the arrival of the signal from the first photodetector with the response of the second, which acts as a sampling gate. If two photodetectors are identical, the measured charge is proportional to the auto-correlation function given by

$$Q(\tau) = \int_{-\infty}^{+\infty} g_1(t)g_2(t+\tau)dt \tag{2.25}$$

where g(t) is the signal from the dc biased photodetector, and τ is the time delay. The signal output from the second photodetector is given by the correlation of the signal from the first one with a time delay. Note that each signal is a convolution of the impulse response of the photodetector, the optical pulse width, and the circuit effects such as the transmission line. The measured time resolution is determined by the response of the two photodetectors and the interconnecting circuitry.



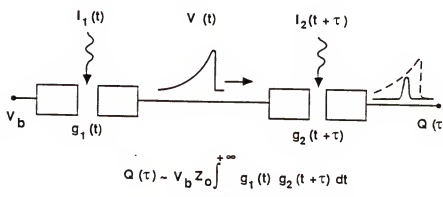


Figure 2.3 Schematic diagrams for the sampling/correlation and for the sampling/double-gap correlation measurements.

2.7.3. Electro-Optical Sampling

This technique, as shown in Fig.2.4, requires a microstrip transmission line deposited on a linear electro-optic crystal such as $LiTaO_3$ [46,47]. A train of picosecond pulses from a mode-locked dye laser is split into two beams. One strikes a photodiode to launch a signal to the transmission line. The other passes transversely through the crystal and its intensity is modulated by the electric field. By varying the relative time delay between the two beams, the temporal resolution of the photodetector response is obtained.

The voltage waveform on the transmission line is a convolution of the photodetector response, the laser pulse width, and the transmission line dispersion. The subsequent sampling is a cross-correlation of the laser pulse with the voltage waveform. The operations of convolution and correlation are associative, and the sampler output is, therefore, equivalent to the convolution of the photodetector impulse response with the auto-correlation of the laser pulse. Since the auto-correlation of the laser pulse is independently measured, its contribution can be deconvolved to extract the photodetector impulse response.

2.7.4. Optical Heterodyne

This technique can measure the bandwidth of a photodetector accurately by using two CW lasers [48,49]. The accuracy is mainly dependent on the bandwidth of the transmission line and the microwave spectrum analyzer. The simple system, shown in Fig.2.5, consists two temperature-tuned semiconductor diode lasers, and the combined beam is incident on the photodiode via a single mode optical fiber. To avoid the frequency instability of the lasers, it is necessary to reduce the optical feedback by the incorporation of an optical isolator.

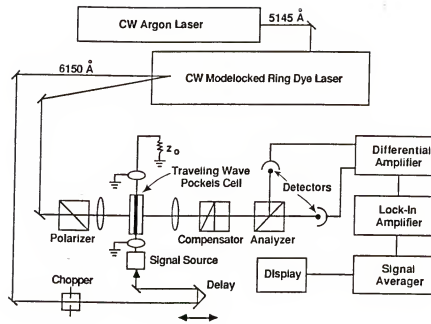


Figure 2.4 Schematic diagram for the electro-optical sampling measurement.

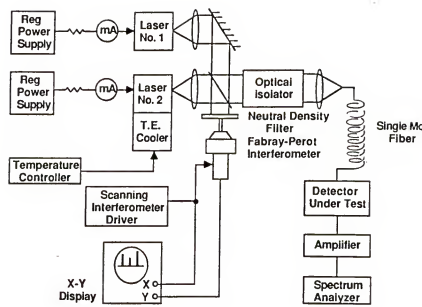


Figure 2.5 Schematic diagram-for the optical heterodying measurement.

CHAPTER THREE
SURFACE PASSIVATION AND ANTIREFLECTION COATING

Studies of surface passivation and antireflection coating on GaAs and $In_{.53}Ga_{.47}As$ interdigitated metal-semiconductor-metal (IMSM) Schottky barrier photodiodes have been made using SiO_2, Si_3N_4, and polyimide films. Current-voltage measurements on these IMSM structures revealed that Si_3N_4 for GaAs and polyimide for $In_{.53}Ga_{.47}As$ yielded the best surface passivation, with the lowest surface leakage current.

3.1. Introduction

Recently there has been considerable interest in understanding the physics and chemistry of interfacial properties between the dielectric films and III-V semiconductors. This is due to the fact that all photonic devices including photodetectors, lasers, light emitting diodes, and solar cells, use the dielectric overlayers for passivation, encapsulation, and antireflection coating. For example, a photodiode with a properly passivated surface shows low leakage current, large breakdown voltage, and higher responsivity. Near zero reflection loss can be achieved in these devices by using an optimum AR coating. In an effort to reduce the leakage current of $In_{.53}Ga_{.47}As$ and InGaAsP/InP p-n junction structures, several investigators [50-52] have reported that plasma-deposited Si_3N_4, polyimide, and SF_6 propelled photoresist, if properly applied, can reduce the leakage current significantly. Capasso and Williams [53] have proposed a plasma hydrogenation in conjunction with nitridization for the passivation of GaAs and other III-V compound semiconductor devices. In this chapter, surface passivation and antireflection coating on the GaAs and $In_{.53}Ga_{.47}As$ back-to-back Schottky barrier photodiodes using SiO_2, Si_3N_4, and polyimide deposited dielectric films have been systematically investigated.

3.2. Stoichiometry of GaAs and InGaAs Surfaces

The calculations and experiments of phase diagram for the Ga-As-O system have demonstrated that the only stable phases that can exist in thermodynamic equilibrium with GaAs are Ga_2O_3 and elemental As [54]. Any As_2O_3 should react with GaAs to form Ga_2O_3 and free As in high temperature thermal oxidation. Low temperature processes can produce a non-equilibrium Ga_2O_3-As_2O_3 surface oxide layer. Both plasma oxides and anodically grown oxides on GaAs contain roughly equal parts of Ga_2O_3 and As_2O_3, without any detectable ($\sim$ 100 Å) free As. A subsequent thermal annealing results in an equilibrium condition via the following reaction

$$As_2O_3 + 2GaAs \rightarrow Ga_2O_3 + 4As \tag{3.1}$$

This reaction occurs spontaneously but slowly, even at room temperature. This indicates that a GaAs surface exposed to air will form a thin ($\sim$ 100 Å) native oxide (As_2O3, Ga_2O_3) and a fraction of a monolayer of free As. This fractional As monolayer is sufficient to increase drastically the surface recombination velocity and surface leakage current. Thus it appears that surface oxidation will lead to the formation of free As, and to the enhanced surface leakage current.

The effect of surface oxidation on GaAs photodiode performance is indirectly explained by the fact that the dark current of the oxygen-rich passivated layers with SiO_2 or Si_3N_4 is much larger than that of the oxygen-free passivated layers. In this respect, one can note that deposition of a dielectric including oxygen (SiO_2), or of oxygen-contaminated Si_3N_4 can cause a buildup of As_2O_3, thus increasing the amount of As. The effect of surface As_2O_3 on GaAs is expected to be the excess leakage current due to the midgap states and/or the long-term failure of device performance (Ga_2O_3 will not produce any surface leakage current because it is a wide bandgap and nonconductive oxide).

The passivation of $In_{.53}Ga_{.47}As$ lattice matched to InP is of particular importance for 1.3 $\sim$ 1.6 μm fiber optic detectors and sources. Based on the thermodynamic arguments,

the stable species expected on the oxidized InGaAs are Ga_2O_3, In_2O_3, and As_2O_3. Among them, Ga_2O_3 has the most negative free energy of formation, and As_2O_3 has the least negative free energy. Thus, Ga_2O_3 and In_2O_3 are expected to be formed preferentially as a stable solid phase upon oxidation of InGaAs surface. However, As_2O_3 can react with the fractional GaAs and InAs by

$$As_2O_3 + 2GaAs \rightarrow Ga_2O_3 + 4As \tag{3.2}$$

$$As_2O_3 + 2InAs \rightarrow In_2O_3 + 4As \tag{3.3}$$

It is important to point out that, at moderate temperature (such as plasma oxidation or anodic oxidation near 300 K), As_2O_3 is also expected to be present on the oxidized surface.

The effect of free As and As_2O_3 on the InGaAs surface is analogous to that of free As on the GaAs surface. Moreover, In_2O_3 is conductive and therefore also likely to cause the surface leakage current. For photodiode applications, the evidenace for the enhancement of leakage current due to the surface oxidation was supported by Susa et al. [55] who found that use of an SiO_2 diffusion mask on InGaAs resulted in anomalously large dark current, which was reduced by stripping off the SiO_2 layer.

3.3. Experiments

The device structures used in this study were the interdigitated metal-semiconductor-metal (IMSM) Schottky barrier photodiodes [56] fabricated on n-GaAs epilayer (N_d = 6×10^{15} cm^{-3}) grown on semi-insulating (S.I.) GaAs substrate by liquid phase epitaxy (LPE), and on p-$In_{.53}Ga_{.47}As$ epilayer ($N_a = 7 \times 10^{16}$ cm^{-3}) grown on S.I. InP substrate by molecular beam epitaxy (MBE). To form back-to-back Schottky barrier contacts, a gold film of 2000 Å was deposited by electron-beam evaporation, and a standard lift-off process was used to make an interdigitated pattern, as shown in Fig.3.1. The Au fingers are 8 μm wide by 200 μm long with an interelectrode spacing of 12 μm. Prior to metal deposition, the wafers were chemically etched in H_2SO_4 followed by HCl to remove As_2O_3-rich surface

oxide films [57]. Subsequently, SiO_2 film was deposited on the samples GaAs-2 and InGaAs-2 by electron-beam evaporation with a deposition rate of 3 Å/sec, and densified at 200 °C for 3 hours in H_2 gas ambient. For the deposition of Si_3N_4 film on the samples GaAs-3 and InGaAs-3, plasma-assisted rf sputtering was used with a deposition rate of 16 Å/min. During the deposition, a liquid nitrogen trap was used to reduce the oxygen contamination from moisture. The thicknesses of SiO_2 and Si_3N_4 were optimized by the quarter wavelength design rule for the maximum transmission of light at a certain wavelength (e.g., 1370 Å of SiO_2 and 1000 Å of Si_3N_4 for GaAs, and 2570 Å and 1870 Å for $In_{.53}Ga_{.47}As$, respectively). A 3 μm thick polyimide (Dupont PI 2555) film, which is transparent to the wavelength of $0.55 \sim 1.7$ μm [52], was spin-coated on the samples GaAs-4 and InGaAs-4, and prebaked at 125 °C (± 3 °C) for 30 min. A final bake was done at 240 °C for one hour in H_2 gas ambient. During the fabrication, heat treatment was restricted below 260 °C to prevent the gallium from dissolving into metal contacts (Au), otherwise resulting in the morphologically irregular contacts with alloy spiking and changes of the Schottky barrier height [58]. The geometric and passivation parameters of GaAs and $In_{.53}Ga_{.47}As$ samples are summarized in Table 3.1.

3.4. Results and Discussion

The current-voltage (I-V) characteristics for both GaAs and $In_{.53}Ga_{.47}As$ IMSM Schottky barrier photodiodes with different passivation films were measured by using HP 4145A, and the results are shown in Fig.3.2 and Fig.3.3, along with the chemically etched (H_2SO_4 followed by HCl) samples. It should be noted that one Schottky barrier contact of the IMSM photodiode is always reverse biased. As a result the current flow in an IMSM photodiode is always limited by the reverse leakage current, and is very sensitive to the surface condition. For the GaAs diodes, except for the SiO_2 passivated one, breakdown voltages were greater than -30 V, and Si_3N_4 was found to be the best passivation film among this group of films studied with a dark current density of 4.45×10^{-6} A/cm^2 at $V_R = -5$ V.

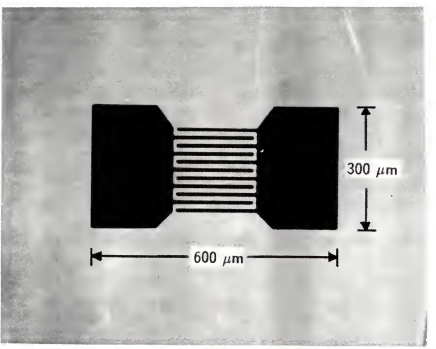


Figure 3.1 Top view of the IMSM Schottky barrier photodiode.

Table 3.1 The geometric and passivation parameters of GaAs and InGaAs samples.

Sample No.	Dopant Density (cm^{-3})	Schottky Metal	Surface Preparation	Passivation
GaAs-1	$N_d = 2.3 \times 10^{16}$	Au	NH_4OH	Bare Surface
GaAs-2	$N_d = 2.3 \times 10^{16}$	Au	NH_4OH	SiO_2
GaAs-3	$N_d = 2.3 \times 10^{16}$	Au	NH_4OH	Si_3N_4
GaAs-4	$N_d = 2.3 \times 10^{16}$	Au	NH_4OH	Polyimide
InGaAs-1	$N_a = 5.0 \times 10^{15}$	Au	H_2SO_4,HCl	Bare Surface
InGaAs-2	$N_a = 5.0 \times 10^{15}$	Au	H_2SO_4,HCl	SiO_2
InGaAs-3	$N_a = 5.0 \times 10^{15}$	Au	H_2SO_4,HCl	Si_3N_4
InGaAs-4	$N_a = 5.0 \times 10^{15}$	Au	H_2SO_4,HCl	Polyimide

On the other hand, breakdown voltages for the $In_{.53}Ga_{.47}As$ diodes were $-6 \sim -7$ V, and diode passivated with a polyimide film showed the best I-V characteristics with dark current density of 7.43×10^{-5} A/cm^2 at $V_R = -5$ V. The relatively larger leakage current density observed in p-$In_{.53}Ga_{.47}As$ (larger than that of n-GaAs) can be partially attributed to the lower schottky barrier height and the different surface stoichiometry [59]. The poor I-V characteristics of SiO_2 passivated GaAs and $In_{.53}Ga_{.47}As$ samples can be explained as follows. Deposition of a dielectric including oxygen (SiO_2) can cause a buildup of As_2O_3 or/and In_2O_3, which are expected to be the source of the excess leakage current and the long-term failure of device performance [53].

Measurements of the spectral responses of GaAs and $In_{.53}Ga_{.47}As$ IMSM photodiodes were carried out in the wavelength range of $0.4 \sim 0.9$ μm and $1.1 \sim 1.7$ μm, respectively. The external quantum efficiency and responsivity of GaAs photodiodes were $\sim$ 72 % and $\sim$ 0.65 A/W, respectively, as shown in Fig.3.4. The results show that using quarter wavelength AR coating can greatly improve the spectral response and responsivity of these photodiodes. Furthermore, the dark current after illumination for three hours was found to be very stable. This is a clear indication of good surface passivation in these photodiodes.

3.5. Conclusion

A systematic study of surface passivation on GaAs and $In_{.53}Ga_{.47}As$ IMSM Schottky barrier photodiodes using SiO_2, Si_3N_4, and polyimide deposited films has been carried out. The results show that Si_3N_4 on GaAs and polyimide on $In_{.53}Ga_{.47}As$ are the most effective dielectric films for reducing the leakage current and reflection loss in these photodiodes.

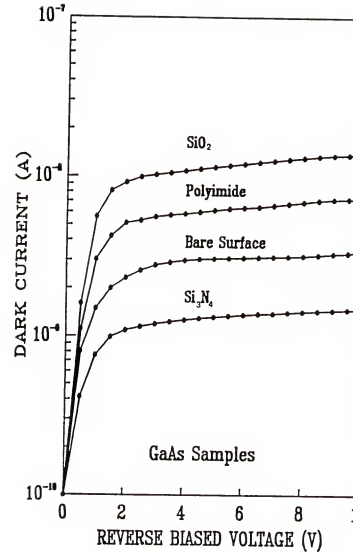


Figure 3.2 Dark currents as a function of reverse-bias voltage for the GaAs IMSM photodiodes passivated with SiO_2, Si_3N_4, polyimide, and bare surface.

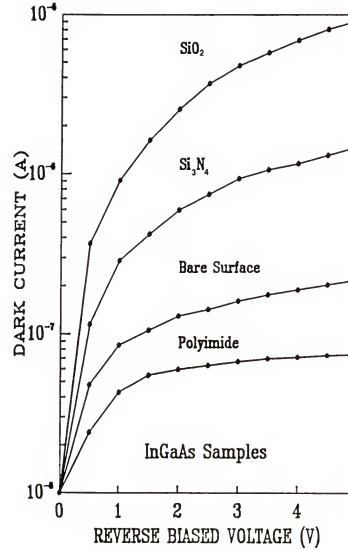


Figure 3.3 Dark currents as a function of reverse-bias voltage for the $In_{.53}Ga_{.47}As$ IMSM photodiodes passivated with SiO_2, Si_3N_4, polyimide, and bare surface.

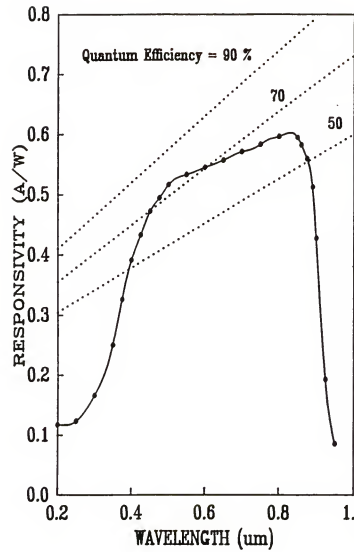


Figure 3.4 Measured external quantum efficiency and responsivity of the GaAs IMSM Schottky barrier photodiodes.

CHAPTER FOUR
DEVELOPMENT OF A HIGH-SPEED PLANAR $GaAs/Al_{0.3}Ga_{0.7}As$ SCHOTTKY BARRIER PHOTODIODE

A high-speed high-sensitivity planar $GaAs/Al_{0.3}Ga_{0.7}As$ heterostructure Schottky barrier photodiode has been designed, fabricated, and characterized. A highly doped $Al_{0.3}Ga_{0.7}As$ buffer layer is used to reduce the series resistance and the undesired diffusion tailing. Furthermore, surface passivation and antireflection coating, with various dielectric films, are performed to reduce the reverse-bias dark current and the relfection loss of the incident light, thereby significantly improving the sensitivity of the photodiode. The measured external quantum efficiency and responsivity are 60% to 77% and 0.47 A/W to 0.6 A/W, respectively, for the wavelength range of 0.5 μm to 0.84 μm. A risetime of 8.5 ps and a 3-dB cutoff frequency of 50 GHz have been measured.

4.1. Introduction

Recently, with the development of femtosecond-pulsed lasers and the modulation of light in the several tens of gigahertz frequency range, photodetectors with high response speed and high sensitivity have become necessary for optical computing and communication systems [2,3]. For such applications, a high-speed photodetector must satisfy several requirements, such as high sensitivity, low dark current, very low capacitance, and low noise, at the operating wavelength. The promising candidates for high-speed photodetectors are Schottky barrier diodes [13-15], p-i-n diodes [4,5], photoconductors [19,20], and APDs [28-30].

A planar Schottky barrier GaAs photodiode is very attractive both for integrated optoelectronic applications and for short optical links in which the maximum data rate is not

limited by the dispersion of optical fibers but by the photodetectors, lasers, and electronic circuitry. In this chapter, a high-speed high-sensitivity GaAs/$Al_{0.3}Ga_{0.7}As$ heterostructure planar Schottky barrier photodiode capable of operating beyond 50 GHz has been designed, fabricated, and characterized.

4.2. Analysis and Design

The main considerations in the design of photodetectors are the response-speed and the sensitivity. The response-speed of the Schottky barrier photodiode can be determined primarily by three parameters; the transit time (t_{tr}) across the depletion region, the diffusion time (t_{diff}) in the quasi-neutral reqion, and the RC time constant (t_{RC}) required to discharge the junction capacitance through a combination of internal and external resistances. For high-speed operation, the Schottky barrier photodiode requires a narrow depletion region for a small transit time, and a wide depletion region and a small area for a low junction capacitance. Therefore, the geometry and dimension of a photodiode as well as the dopant density of the epilayer should be optimized for the high-speed and high-sensitivity operation. The physical parameters of GaAs material are summarized in Table 4.1.

The cross sectional and top views of the designed GaAs/$Al_{0.3}Ga_{0.7}As$ planar Schottky barrier photodiode are shown in Fig.4.1. This planar geometry on the semi-insulating GaAs substrate can reduce the parasitic capacitance significantly; it is also suitable for integrated optoelectronic circuits. To reduce the series resistance, a thin (0.3 μm) heavily doped (1×10^{18} cm^{-3}) n^+- buffer layer is used. In addition, to eliminate the undesirable absorption in this layer, which results in a long diffusion time, an $Al_{0.3}Ga_{0.7}As$ layer, transparent to the wavelength of interest, can be used to replace the n^+-GaAs buffer layer. The undoped (5×10^{15} cm^{-3}) n-GaAs layer (1 μm) is used as the absorption layer. The illumination window is formed by a thin (100 Å) transparent Au film with a diameter of 6 μm. The small window area and the n^+-$Al_{0.3}Ga_{0.7}As$ buffer layer can significantly reduce the RC time constant and the diffusion time, resulting in improvement of the response speed of the

Table 4.1 Physical parameters of GaAs material at 300 K [60].

Energy Bandgap (eV)	E_g=1.43
Dielectric Constant	ϵ_s=13.1
Mobility (cm^2/V-s)	μ_n=8500
	μ_p=400
Diffusion Constant (cm^2/s)	D_n=90
	D_p=5
Diffusion Length (μm)	L_n=5 (p-type GaAs)
	L_p=2 (n-type GaAs)
Effective Mass	m_n^*=0.068 m_o
	m_{pl}^*=0.082 m_o
	m_{ph}^*=0.45 m_o
Intrinsic Carrier Density (cm^{-3})	$n_i = 1.79 \times 10^6$
Effective Density of States (cm^{-3})	$N_c = 4.7 \times 10^{17}$
	$N_v = 7.0 \times 10^{18}$
Effective Richardson Constant ($Acm^{-2}K^{-2}$)	A^*=120

photodiode. The calculated device performances versus device parameters are summarized in Table 4.2.

To improve the sensitivity of a photodiode, i.e., the minimum detectable power level of an incident light, the dark current and reflection loss should be minimized. It is known, however, that a GaAs surface exposed to air will form a thin native oxide (Ga_2O_3 and As_2O_3) and a fraction of a monolayer of free elemental As, which increase the surface leakage current due to the midgap states, and causes the long term failure of device performace. Hence, surface passivation is necessary to reduce the reverse-bias dark current of a photodiode. Various dielectric films such as SiO_2, Si_3N_4, and polyimide are used for surface passivation. In addition, these dielectric films can be served as an antireflection (AR) coating, of which the thickness should be optimized with the quarter wavelength design rule [34] for the maximum transmission of light.

4.3. Fabrication

A high-speed planar Schottky barrier photodiode has been fabricated on n^--GaAs/n^+-$Al_{0.3}Ga_{0.7}As$ epilayers grown on (100) oriented semi-insulating GaAs substrate by liquid phase epitaxy (LPE). The n^--GaAs and n^+-$Al_{0.3}Ga_{0.7}As$ epilayers with thicknesses of 1.5 and 0.3 μm have dopant densities of 5.0×10^{15} and 2.0×10^{18} cm^{-3}, respectively. The Schottky barrier and ohmic contacts were formed by using a standard lift-off process. The ohmic contact was first formed by deposition of Au-Ge/Ni alloy metal, and by subsequent annealing at 450 °C for 120 sec. in H_2-N_2 (5-95 %) forming gas ambient. A 100 Å Au film for a transparent Schottky barrier contact and a 200/3000 Å Cr/Au film for a bonding pad were deposited by electron-beam evaporation at a deposition rate of 2 Å/sec at a pressure of 8.0×10^{-7} Torr. For the surface passivation and antireflection coating, SiO_2 (1400 Å) and Si_3N_4 (1100 Å) were deposited either by electron-beam evaporation or by plasma-assisted rf sputtering. A 2.5 μm thick polyimde (DuPont PI 2555), which is transparent to the wavelength of interest, was spin-coated onto the wafer. Detailed fabrication procedures are

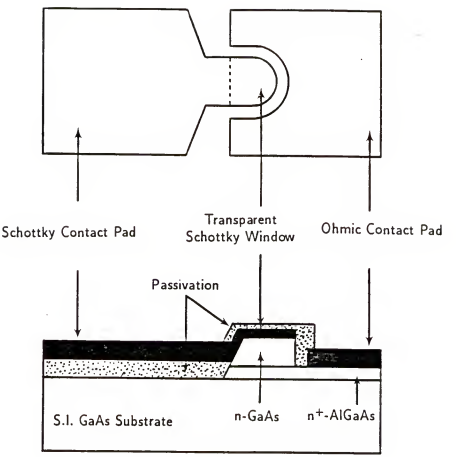


Figure 4.1 Schematic diagram of the planar $GaAs/Al_{0.3}Ga_{0.7}As$ Schottky barrier photodiode.

Table 4.2 Designed device parameters, calculated response speed, and quantum efficiency of the planar $GaAs/Al_{0.3}Ga_{0.7}As$ Schottky barrier photodiode.

Device Parameters	n-GaAs/n^+-AlGaAs		
Epilayer Thickness (μm)	1.0/0.3		
Doping Concentration (cm^{-3})	$5 \times 10^{15}/1 \times 10^{18}$		
Diameter of Active Area (μm)	6	10	20
Junction Capacitance (fF)	2.80	7.79	3.12
Series Resistance (Ω)	182.32	109.39	54.79
RC Time (ps)	3.65	5.24	8.26
Drift Time (ps)	3.57		
Diffusion Time (ps)	2.53		
Total Time (ps)	5.69	6.83	9.35
Cutoff Frequency (GHz)	58.6	48.8	35.6
Quantum Efficiency (%)	66		

listed in Table 4.3. For the characterization of the fabricated photodiodes, test samples were mounted either on a microstrip line or on a coplanar waveguide. The universal test fixture with a 50 Ω microstrip is illustrated in Fig.4.2.

4.4. Results and Discussion

Current-voltage (I-V) characteristics of the fabricated planar $GaAs/Al_{0.3}Ga_{0.7}As$ Schottky barrier photodiodes were measured by using HP 4140B pA Meter/DC Voltage Source. The photodiode passivated with Si_3N_4 showed the best I-V characteristics, and is shown in Fig.4.3. The reverse-bias dark current density was 1.3×10^{-7} A/cm^2, at $V_R = -5$ V and the breakdown voltage was found to be around -30 V at 10 μA of dark current. The ideality factor, determined from the slope of forward-bias I-V characteristics, was between 1.11 to 1.21. Capacitance-voltage (C-V) characteristics were measured by using HP 4280A C-Meter/C-V Plotter. The total (junction and parasitic) capacitances of the photodiode with an area of 9.8×10^{-5} cm^2 were less than 10 fF at $V_R = -5$ V.

The spectral response of the fabricated photodiode was measured by using Jarrell-Ash 82-410 Quarter-Meter Monochromator. The radiation from MK-II fiber light-source was focused on the entrance slit of the monochromator. The optical power was measured by using Optics Technology M-615 Optical Power Meter, and normalized by the area of the light spot to obtain the equivalent optical power. The quantum efficiency and responsivity of the photodiode were calibrated by using Spectra Physics Model-120 He-Ne laser. As is shown Fig.4.4, the measured external quantum efficiency and responsivity of the Si_3N_4 coated photodiode were $60 \sim 77$ % and $0.47 \sim 0.6$ A/W, respectively, for the wavelength range of $0.5 \sim 0.84$ μm.

The response speed of the photodiode can be directly measured in the time domain either by impulse response or by sampling/correlation. For the impulse response measurement, Nd:Yag laser (wavelength of 0.53 μm, pulse width of 50 ps, and repetition rate of 80 MHz) and Tektronix 7844 Sampling Scope with S-6 sampling head (risetime of 30 ps)

Table 4.3 Fabrication procedures for the planar GaAs/$Al_{0.3}Ga_{0.7}As$ Schottky barrier photodiode.

1. Starting material is n-GaAs/n^+-$Al_{0.3}Ga_{0.7}As$ epilayers grown on semi-insulating GaAs substrate by LPE.
2. Clean and degrease wafer with TCE, acetone, methanol under ultrasonic agitation, and rinse with D.I.water followed by blowing dry with N_2 and baking at 90 °C to drive off any residual water vapor.
3. Prebake at 120 °C for 20 min.
4. Spin on positive photoresist (Shipley AZ 1400-13) at 5000 rpm for 40 sec.
5. Softbake wafer at 90 °C for 25 min.
6. Align it to contact mask and expose to UV light for 20 sec.
7. Develop positive photoresist using Shipley developer (MF-351:D.I.water=1:5).
8. Perform wet chemical etching just before metal deposition to remove native oxides from the surface of contact area ($HF:H_2O$:1:5 or HCl).
9. Deposit metal film (Au-100 Å for a transparent Schottky contact, Cr/Au-200/3000 Å for a Schottky bonding pad, and Au-Ge/Ni/Au-1000/300/2000 Å for ohmic contact) by electron-beam evaporation at a pressure of less than 10^{-6} Torr and at a deposition rate of 2 Å/sec.
10. Remove unwanted metal film with photoresist by ultrasonic agitation in acetone.
11. Alloy at 450 °C for 120 sec. in H_2-N_2 (5-95 %) forming gas ambient for ohmic contact.
12. Deposit Si_3N_4 (2000 Å) for the surface passivation and antireflection coating by plasma-assisted rf sputtering at a deposition rate of 16 Å/min.
13. Open windows for the ohmic and Schottky contact pad areas by etching Si_3N_4 in HF solution.

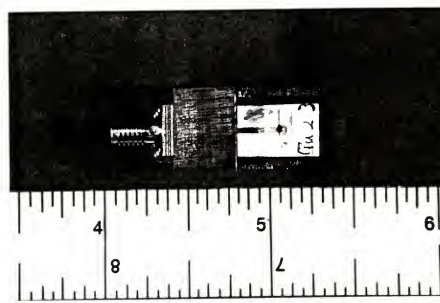


Figure 4.2 Fabricated planar GaAs/$Al_{0.3}Ga_{0.7}As$ Schottky barrier photodiode on the universal test fixture with a 50 Ω microstrip line.

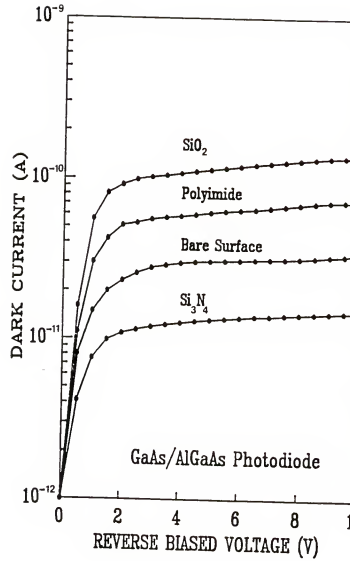


Figure 4.3 Current-voltage characteristics of the planar GaAs/$Al_{0.3}Ga_{0.7}As$ Schottky barrier photodiode.

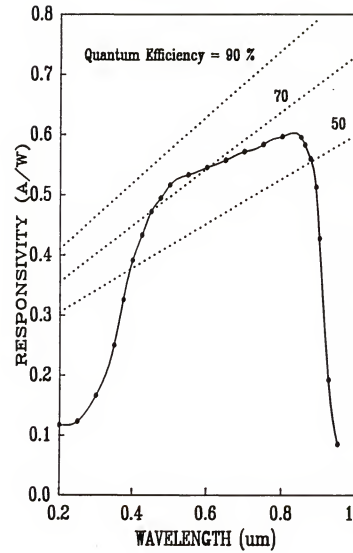


Figure 4.4 External quantum-efficiency and responsivity of the planar $GaAs/Al_{0.3}Ga_{0.7}As$ Schottky barrier photodiode.

were used. Figure 4.5 shows the measured impulse response with a risetime of 43 ps. It should be noted that the measured risetime was attributed mainly to the time delay of the sampling head and the external circuitry.

For the sampling/correlation measurement, the photodiodes were mounted on the test fixture of coplanar waveguide lines. As an optoelectronic sampling gate (Auston switch) [44], a photoconductive circuit element (PCE) of a 10 μm gap between the signal line and sampling line was formed on the semi-insulating GaAs substrate. Figure 4.6 illustrates the schematic diagram of the coplanar waveguide test fixture used in this measurement. A dispersion-compensated [61] colliding-pulse mode-locked ring dye laser [62] (FWHM of 80 fs, wavelength of 620 nm, and repetition rate of 125 MHz) was used for photoexcitation of the photodiode and the sampler PCE. The delay between the two laser pulses incident on the photodiode and on the sampler was continuously varied over 670 ps by a stepping motor driven translation stage. The sampled signals were fed into a lock-in amplifier (PAR 124A with PAR 184 Current Sensitive Preamp) that was phase-locked with a light chopper (PAR 125A). Data acquisition was done by averaging at the rate of 50 points per second. Figure 4.7 shows the measured response speed of the photodiode. A risetime of 8.5 ps and a FWHM of 16 ps were measured. This value is compatible to the 3-dB cutoff frequency of 50 GHz.

4.5. Conclusion

A high-speed high-sensitivity planar GaAs/AlGaAs heterostructure Schottky barrier photodiode has been designed, fabricated, and characterized. Highly doped $Al_{0.3}Ga_{0.7}As$ buffer layer is used to reduce the series resistance and the undesired diffusion tailing. Furthermore, surface passivation and antireflection coating, with various dielectric films, are performed to reduce the reverse-bias dark current and the relfection loss of incident light, thereby significantly improving the sensitivity of a photodidoe. The measured external quantum efficiency and responsivity are $60 \sim 77$ % and $0.47 \sim 0.6$ A/W, respectively, for

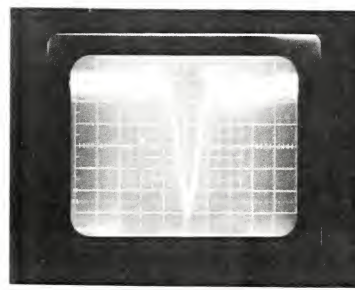
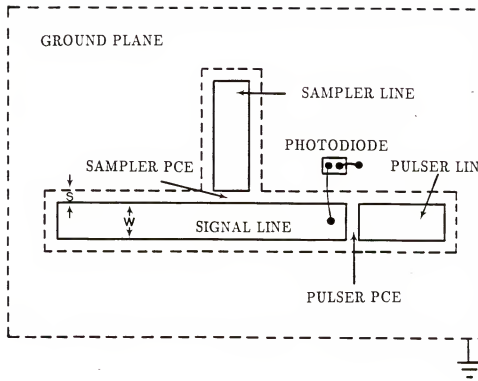


Figure 4.5 Impulse response of the planar $GaAs/Al_{0.3}Ga_{0.7}As$ Schottky barrier photodiode.



PCE GAP = 10 μm
SAMPLER LINE WIDTH (W) = 60 μm
CENTER LINE - GROUND PLANE SPACING (S) = 30 μm
SAMLPER LINE LENGTH = 2 mm
PULSER LINE LENGTH = 2 mm
SIGNAL LINE LENGTH = 10 mm
PULSER - SAMPLER SPACING = 2 mm

Figure 4.6 Schematic diagram of the coplanar waveguide test fixture used in the sampling/correlation measurement.

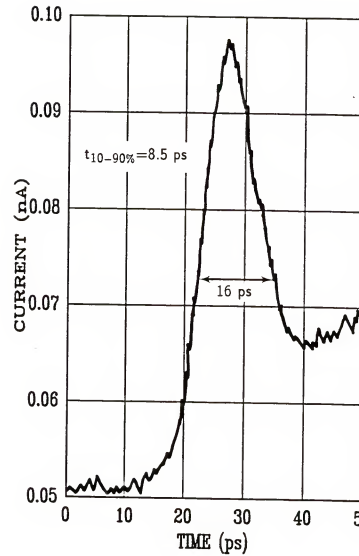


Figure 4.7 Response speed of the planar $GaAs/Al_{0.3}Ga_{0.7}As$ Schottky barrier photodiode by using sampling/correlation.

the wavelength range of $0.5 \sim 0.84\ \mu$m. The sampling/correlation measurements show that the risetime of the photodiode is 8.5 ps, corresponding to the 3-dB cutoff frequency of 50 GHz.

CHAPTER FIVE
DEVELOPMENT OF A PLANAR $In_{.53}Ga_{.47}As$ BACK-TO-BACK SCHOTTKY BARRIER PHOTODIODE

A high-speed planar back-to-back Schottky barrier photodiode on p-$In_{.53}Ga_{.47}As/p^+$-InP/semi-insulating InP substrate has been designed, fabricated, and characterized. The measured external quantum efficiency and responsivity of the photodiode passivated with a polyimide film are $48 \sim 69$ % and $0.49 \sim 0.56$ A/W, respectively, for the wavelength range of $0.9 \sim 1.8$ μm. The 3-dB cutoff frequency of 2.7 GHz is determined from the equivalent circuits.

5.1. Introduction

A high-speed and high-sensitivity photodetector operating in the infrared regime, especially close to the dispersion minimum of optical fibers ($1.30 \sim 1.55$ μm), are of great interest for lightwave communications. $In_{.53}Ga_{.47}As$, a direct bandgap semiconductor ($E_g = 0.75$ eV at 300 K), is one of the most suitable materials for photodetector applications in the near infrared. Another attractive feature of $In_{.53}Ga_{.47}As$ is that single crystal films of this composition can be grown directly on InP substrates using any of the major epitaxial growth techniques.

To date, most of effort has been directed toward development of mesa-type p-i-n photodiodes [9,10,12] and APDs [30,31]. For the applications to monolithically integrated optoelectronic circuits, however, a planar Schottky barrier photodiode is of interest due to the simplicity of fabrication and integration. In this chapter, a new planar $In_{.53}Ga_{.47}As$ back-to-back Schottky barrier photodiode has been designed, fabricated, and characterized.

5.2. Analysis and Design

The main considerations in the design of photodetectors are response-speed and responsivity. For high-speed operation, the geometry and dimension of a photodiode as well as the dopant density of the epilayer should be optimized for the high-speed and high-sensitivity operation. The physical parameters of $In_{.53}Ga_{.47}As$ material are summarized in Table 5.1.

The cross sectional and top view of the proposed Schottky barrier photodiode is shown in Fig.5.1. To reduce the series resistance, a thin (0.3 μm) heavily doped (1×10^{18} cm^{-3}) p^+ buffer layer is introduced. In addition, to prevent the undesirable absorption in this layer, which results in a long diffusion time, the InP layer, transparent to the wavelength of interest, can be used to replace the $In_{.53}Ga_{.47}As$ layer. As an absorption layer, the undoped (5×10^{15} cm^{-3}) p-InGaAs layer (1 μm) is used. The illumination window is formed by a thin (100 Å) transparent Au film with a diameter of 6 to 20 μm. The small window area and the p^+-InP layer as a buffer layer can reduce the RC time constant and the diffusion time quite significantly. As a result, the response speed of this photodiode is limited by the transit time, which is the ultimate device speed limitation. The Schottky contact pad on the passivated surface will be formed to reduce the stray capacitance and the dark current. The calculated device performaces versus device parameters are summarized in Table 5.2.

5.3. Fabrication

A high-speed planar $In_{.53}Ga_{.47}As$ back-to-back Schottky barrier photodiode has been fabricated on p-$In_{.53}Ga_{.47}As$/p^+-InP epilayers grown on semi-insulating InP substrate of (100) orientation by metal organic chemical vapor deposition (MOCVD). The dopant densities of p-$In_{.53}Ga_{.47}As$ (1 μm) and p^+-InP (0.3 μm) epilayers are 5×10^{15} cm^{-3} and 3×10^{18} cm^{-3}, respectively. The back-to-back Schottky barriers were formed by using a standard lift-off process. A 100 Å Au film for a transparent Schottky barrier contact and a 200/3000 Å Cr/Au film for a bonding pad were deposited by electron-beam evaporation with a deposition rate of 2 Å/sec at a pressure of 8.0×10^{-7} Torr. Finally, for the surface passivation

Table 5.1 Physical parameters of $In_{.53}Ga_{.47}As$ material at 300 K [63].

Energy Bandgap (eV)	E_g=0.75
Dielectric Constant	ϵ_s=12.0
Mobility (cm^2/V-s)	$\mu_n = 1.0 \times 10^4$ $\mu_p = 2.0 \times 10^2$
Diffusion Constant (cm^2/s)	D_n=260 D_p=5.2
Diffusion Length (μm)	L_n=2.28 (p-type InGaAs) L_p=0.32 (n-type InGaAs)
Effective Mass	m_n^*=0.041 m_o m_{pl}^*=0.050 m_o m_{ph}^*=0.49 m_o
Intrinsic Carrier Density (cm^{-3})	$n_i = 7.1 \times 10^{11}$
Effective Density of States (cm^{-3})	$N_c = 2.09 \times 10^{17}$ $N_v = 8.90 \times 10^{18}$
Effective Richardson Constant ($Acm^{-2}K^{-2}$)	A^*=4.92 (n-type InGaAs) A^*=61.9 (p-type InGaAs)

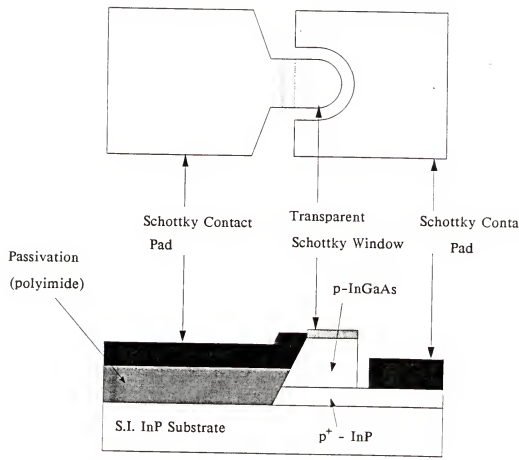


Figure 5.1 Schematic diagram of the planar $In_{.53}Ga_{.47}As$ back-to-back Schottky barrier photodiode.

Table 5.2 Designed device parameters, calculated response speed, and quantum efficiency of the planar $In_{.53}Ga_{.47}As$ back-to-back Schottky barrier photodiode.

Device Parameters	p-$In_{.53}Ga_{.47}As$/p^+-InP		
Epilayer Thickness (μm)	1.0/0.3		
Doping Concentration (cm^{-3})	$5 \times 10^{15}/1 \times 10^{18}$		
Diameter of Active Area (μm)	6	10	20
Junction Capacitance (fF)	2.80	7.79	3.12
Series Resistance (Ω)	169.2	89.7	37.9
RC Time (ps)	5.89	7.97	10.61
Drift Time (ps)	2.75		
Diffusion Time (ps)	2.13		
Total Time (ps)	6.84	8.69	11.16
Cutoff Frequency (GHz)	48.73	38.35	29.86
Quantum Efficiency (%)	78		

and antireflection coating, a 5000 Å polyimide film was spin-coated. Detailed fabrication procedures for the planar $In_{.53}Ga_{.47}As$ back-to-back Schottky barrier photodiode are listed in Table 5.3.

5.4. Results and Discussion

Current-voltage (I-V) characteristics were measured by using HP 4140B pA Meter/DC Voltage Source, and shown in Fig.5.2. The reverse-bias leakage current was 1.3×10^{-6} A, at V_R=-4 V and the breakdown voltage was found to be around -6 V at 10 μA of dark current. The ideality factor determined from the slope of forward I-V characteristics was between 1.17 to 1.26. Capacitance-voltage (C-V) characteristics were measured by using HP 4280A C-Meter/C-V Plotter. The total (junction and parasitic) capacitances of the sample with an area of 9.8×10^{-5} cm^2 were $\sim$ 1 pF at V_R=-5 V. It is believed that the large values of leakage current and capacitance are due to the insufficient Schottky barrier height on p-$In_{.53}Ga_{.47}As$.

The spectral response of the fabricated photodiode is shown Fig.5.3. The external quantum efficiency and the responsivity of the photodiode were 48 $\sim$ 69 % and 0.49 $\sim$ 0.56 A/W, respectively, for the wavelength range of 0.9 $\sim$ 1.8 μm.

The response speed of the planar $In_{.53}Ga_{.47}As$ back-to-back Schottky barrier photodiode can be determined from the RC time constant of the measured equivalent circuits. The circuit parameters were measured by using HP 8510A Network Analyzer, and is shown in Fig.5.4. The 3-dB cutoff frequency is

$$f_{3-dB} = \frac{1}{2\pi(R_s + R_L)C_j} = 2.7\text{GHz} \tag{5.1}$$

5.5. Conclusion

A planar $In_{.53}Ga_{.47}As$ back-to-back Schottky barrier photodiode has been designed, fabricated, and characterized. Highly doped p^+-InP buffer layer is introduced to reduce the

Table 5.3 Fabrication procedures for the planar $In_{.53}Ga_{.47}As$ back-to-back Schottky barrier photodiode.

1. Starting material is p-$In_{.53}Ga_{.47}As/p^+$-InP epilayers grown on semi-insulating InP substrate by MOCVD.
2. Clean and degrease wafer with TCE, acetone, methanol under ultrasonic agitation, and rinse with D.I.water followed by blowing dry with N_2 and baking at 90 °C to drive off any residual water vapor.
3. Prebake at 120 °C for 20 min.
4. Spin on positive photoresist (Shipley AZ 1400-13) at 5000 rpm for 40 sec.
5. Softbake wafer at 90 °C for 25 min.
6. Align it to contact mask and expose to UV light for 20 sec.
7. Develop positive photoresist using Shipley developer (MF-351:D.I.water=1:5).
8. Perform wet chemical etching just before metal deposition to remove native oxides from the surface of contact area ($HF:H_2O$:1:5 or HCl).
9. Deposit metal film (Au-100 Å for a transparent Schottky contact, Cr/Au-200/3000 Å for a Schottky bonding pad by electron-beam evaporation at a pressure of less than 10^{-6} Torr and at a deposition rate of 2 Å/sec.
10. Remove unwanted metal film with photoresist by ultrasonic agitation in acetone.
11. Spin-on polyimide film (5000 Å) for the surface passivation and antireflection coating.
12. Open windows for the bonding pad areas by etching polyimide film in photoresist developer.

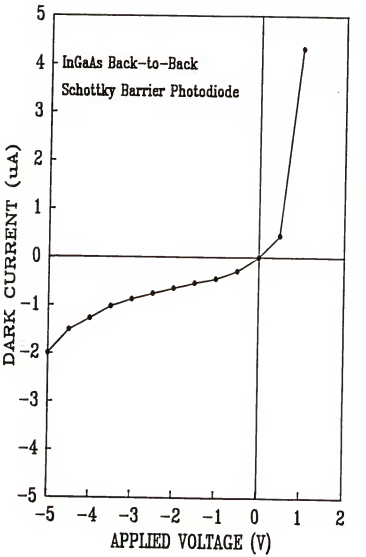


Figure 5.2 Current-voltage characteristics of the planar $In_{.53}Ga_{.47}As$ back-to-back Schottky barrier photodiode.

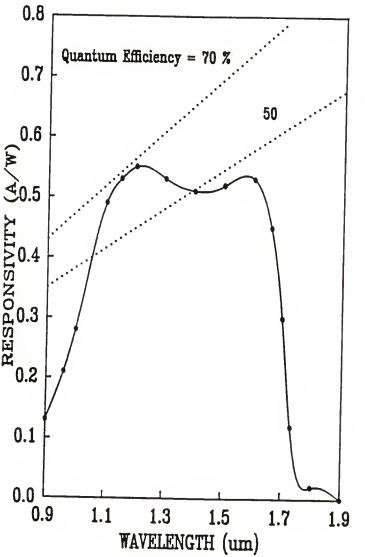
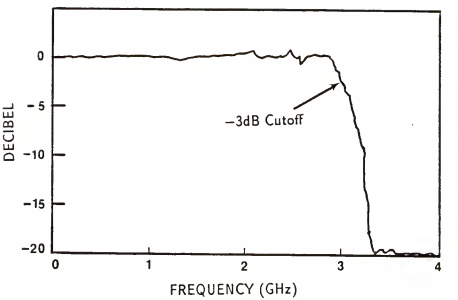
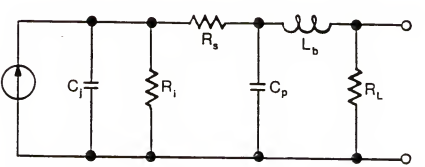


Figure 5.3 External quantum efficiency of the planar $In_{.53}Ga_{.47}As$ back-to-back Schottky barrier photodiode.





$C_j = 0.3$ pF $C_p = 0.04$ pF $L_b = 0.68$ nH

$R_i = 11\,K\Omega$ $R_s = 117\,\Omega$ $R_L = 50\,\Omega$

Figure 5.4 Equivalent circuit model and 3-dB cutoff frequency of the planar $In_{.53}Ga_{.47}As$ back-to-back Schottky barrier photodiode.

series resistance and the undesired diffusion tailing. Furthermore, surface passivation and antireflection coating with a polyimide film have been performed to reduce the reverse-bias dark current and the reflection loss of the incident light, which significantly improve the sensitivity of the photodiode. The measured external quantum efficiency and responsivity are 48 $\sim$ 69 % and 0.49 $\sim$ 0.56 A/W, respectively, for the wavelength range of 0.9 $\sim$ 1.84 μm. The 3-dB cutoff frequency of 2.7 GHz is determined from the equivalent circuit model.

CHAPTER SIX
ENHANCEMENT OF SCHOTTKY BARRIER HEIGHT OF N-$In_{.53}Ga_{.47}As$ USING A NOVEL GRADED-SUPERLATTICE OF $In_{.53}Ga_{.47}As$/ $In_{.52}Al_{.48}As$

Enhancement of the effective Schottky barrier height of n-$In_{.53}Ga_{.47}As$ by means of a thin graded-superlattice of $In_{.53}Ga_{.47}As/In_{.52}Al_{.48}As$ grown by molecular beam epitaxy (MBE) is reported for the first time. Overall effective Schottky barrier heights of $\sim$ 0.71 and $\sim$ 0.60 eV for Au and Cr, respectively, with excellent current-voltage and capacitance-voltage characteristics are obtained. This novel graded-superlattice can circumvent a pile-up of carriers associated with abrupt heterointerface, and hence is advantageous for high-speed electronic and optoelectronic device applications.

6.1. Introduction

It is known that, when compared to GaAs, $In_{.53}Ga_{.47}As$ lattice matched to InP offers superior electrical and optical properties such as high low-field mobility, high saturation velocity, and energy band gap (0.74 eV) for 1.3 $\sim$ 1.65 μm optical fiber communications [12,63,64]. Applications of $In_{.53}Ga_{.47}As$ for metal semiconductor field effect transistors (MESFETs) and Schottky barrier photodiodes, however, have been limited due to the inherently low Schottky barrier height ($\sim$ 0.2 eV) and correspondingly large leakage current [65]. To overcome this problem, several workers have enhanced the effective Schottky barrier height of n-type $In_{.53}Ga_{.47}As$ using various structures. Morgan and Frey [66] used a thin interfacial SiO_x layer to reduce the reverse leakage current. Barnard et al.[67] used a high sheet resistance n-$In_{.52}Al_{.48}As$ layer to form an enhanced Schottky barrier gate for an $In_{.53}Ga_{.47}As$ MESFET. Subsequently, Chen et al.[68] reported an effective barrier height of 0.47 eV using a thin p^+-$In_{.53}Ga_{.47}As$ layer. More recently, Chen et al.[69] used a lattice-mismatched GaAs gate for $In_{.53}Ga_{.47}As$ MESFET. In this chapter, a new technique to

enhance the effective Schottky barrier height of n-$In_{.53}Ga_{.47}As$ through the use of a graded-superlattice of $In_{.53}Ga_{.47}As/In_{.52}Al_{.48}As$ is reported for the first time.

6.2. Experiments

It is known that $In_{.52}Al_{.48}As$ lattice matched to InP and $In_{.53}Ga_{.47}As$ has a direct band gap of 1.47 eV [70] and a high Schottky barrier height of 0.82 eV [71]. A schematic diagram of the test structure grown by molecular beam epitaxy (MBE) is shown in Fig.6.1. The graded-superlattice on top of n-$In_{.53}Ga_{.47}As$ (1.5 μm, 5×10^{15} cm^{-3}) consists of alternated ultrathin multilayers of $In_{.53}Ga_{.47}As$ (n $\sim 5 \times 10^{15}$ cm^{-3}) and $In_{.52}Al_{.48}As$ (n $\sim 5 \times 10^{15}$ cm^{-3}). The duty factors of $In_{.53}Ga_{.47}As$ and $In_{.52}Al_{.48}As$ layers were gradually varied from 5 Å to 55 Å for 10 periods of superlattice. This graded-superlattice is almost same as the pseudo-quaternary GaInAsP semiconductor [72] except that the $In_{.52}Al_{.48}As$ layers were used instead of InP layers. The n^+-$In_{.53}Ga_{.47}As$ buffer layer (0.5 μm, 1×10^{18} cm^{-3}) was introduced to prevent the rectification at the interface of n^+-InP substrate and n-$In_{.53}Ga_{.47}As$ [68]. The ohmic contact was formed on the n^+-InP substrate by evaporating Au-Ge/Ni/Au and by alloying at 450 °C for 30 sec. The Schottky barrier contact was formed on top of the graded-superlattice by evaporating Au (or Cr). A mesa-etch with a H_3PO_4:H_2O_2:H_2O (1:1:38) solution was used for device isolation.

6.3. Results and Discussion

The resultant effective band gap of the graded-superlattice is spatially graded between $In_{.53}Ga_{.47}As$ (0.74 eV) and $In_{.52}Al_{.48}As$ (1.47 eV), and can be expressed as [72]

$$E_g^{eff} = \frac{E_g(In_{.53}Ga_{.47}As) \cdot L(In_{.53}Ga_{.47}As) + E_g(In_{.52}Al_{.48}As) \cdot L(In_{.52}Al_{.48}As)}{L(In_{.53}Ga_{.47}As) + L(In_{.52}Al_{.48}As)} \quad (6.1)$$

where the L is the layer thickness. By the same manner, the effective Schottky barrier height of the graded-superlattice can be considered to be spatially graded between $In_{.53}Ga_{.47}As$ (0.2 eV) and $In_{.52}Al_{.48}As$ (0.82 eV), and can be approximated by

$$\phi_{Bn}^{eff} = \frac{\phi_{Bn}(In_{.53}Ga_{.47}As) \cdot L(In_{.53}Ga_{.47}As) + \phi_{Bn}(In_{.52}Al_{.48}As) \cdot L(In_{.52}Al_{.48}As)}{L(In_{.53}Ga_{.47}As) + L(In_{.52}Al_{.48}As)} \quad (6.2)$$

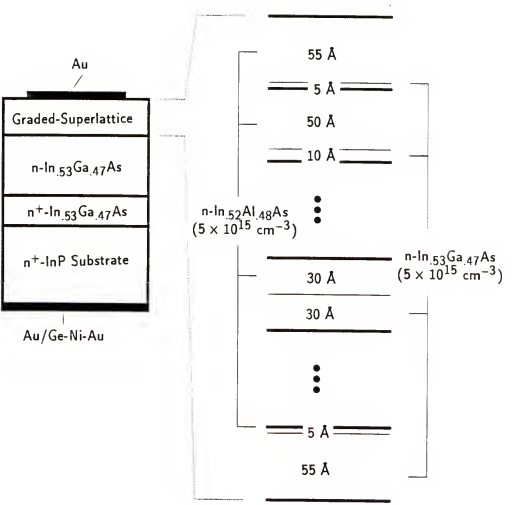


Figure 6.1 Schematic diagram of the Schottky barrier diode of n-$In_{.53}Ga_{.47}As$ using a novel graded-superlattice of $In_{.53}Ga_{.47}As/In_{.52}Al_{.48}As$ grown by MBE. (1 period=60 Å)

Current-voltage (I-V) characteristics of the Au/graded-superlattice/n-$In_{.53}Ga_{.47}As$ Schottky barrier diode with a diameter of 100 μm are shown in Fig.6.2. A breakdown voltage of $-13 \sim -14$ V, a reverse leakage current of 25 nA at -5 V, and an ideality factor, n, of 1.19 were measured. The effective Schottky barrier height, ϕ'_{Bn} can be determined from the following expression [39]

$$\phi'_{Bn} = (\frac{k_B T}{q}) \ln(\frac{A^* T^2}{J_s}) \tag{6.3}$$

where $A^* (= 4\pi q m^* k_B^2/h^3)$ is the Richardson constant for the thermionic emission, and J_s is the reverse saturation current density. From Fig.6.3 and Eq.(6.3), the effective Schottky barrier heights for Au and Cr were determined to be 0.71 and 0.60 eV, respectively. The value of the Richardson constant was taken to be 7.03 $A/cm^{-2} \cdot K^2$ by assuming that the average electron effective mass of the graded-superlattice was $0.06m_o$ ($m_e^* = 0.042m_o$ for $In_{.53}Ga_{.47}As$ and $m_e^* = 0.078m_o$ for $In_{.52}Al_{.48}As$) [70].

Capacitance-voltage (C-V) characteristics of the Au/graded-superlattice/n-$In_{.53}Ga_{.47}As$ Schottky barrier diode were measured at 1 MHz, and no hysteresis was observed. A junction capacitance of 0.32 pF at -5 V was measured for a junction area of 2.0×10^{-5} cm^{-2}. The effective Schottky barrier height can also be determined from the $1/C^2$ versus reverse bias voltage plot (Fig.6.4) and the following equation [39]

$$\phi'_{Bn} = V_i + V_n + \frac{k_B T}{q} \tag{6.4}$$

where V_i is the voltage intercept, and V_n is the potential difference between the Fermi level and the conduction band. By neglecting the image lowering effect, the effective Schottky barrier height of 0.72 eV was determined.

The I-V and C-V characteristics of the Au/graded-superlattice/n-$In_{.53}Ga_{.47}As$ Schottky barrier diode have shown that a barrier height enhancement of ~ 0.51 eV, resulting in an overall effective barrier height of ~ 0.71 eV. Furthermore, another important advantage of the graded-superlattice over the conventional thin semi-insulating $In_{.52}Al_{.48}As$ layer is applicability to high speed electronic and optoelectronic devices, such as MESFETs and Schottky

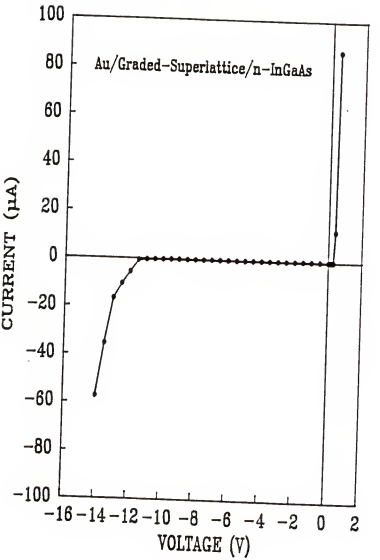


Figure 6.2 Current-voltage characteristics of the Au Schottky barrier diode of a graded-superlattice.

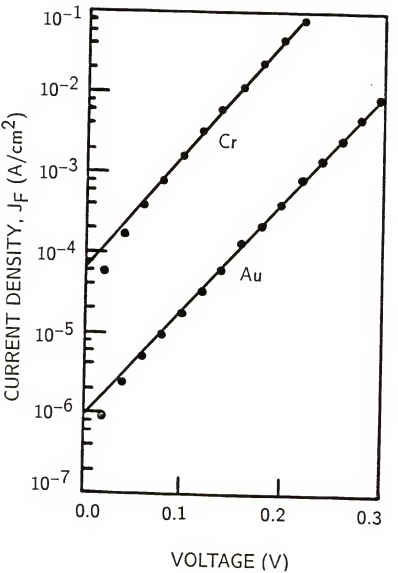


Figure 6.3 Forward-bias current densities and saturation current densities of the Au and Cr Schottky barrier diodes of a graded-superlattice.

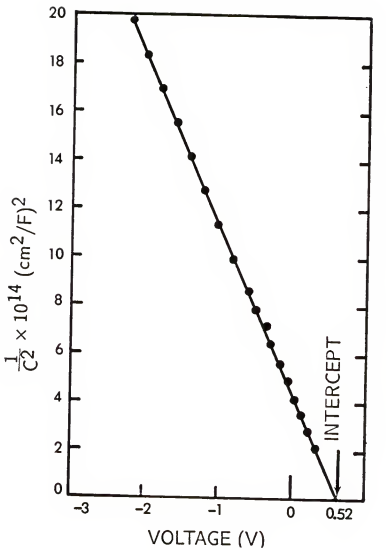


Figure 6.4 $1/C^2$ versus reverse bias voltage plot of the graded-superlattice Schottky barrier diode.

barrier photodiodes. It is known that a pile-up of carriers at the interface of conventional high-low heterojunction, e.g., $In_{.53}Ga_{.47}As/InP$ and $In_{.53}Ga_{.47}As/In_{.52}Al_{.48}As$, degrades the performance of high speed devices [72]. However, the graded-superlattice can smooth out the trapping effect by grading the large band gap discontinuity of $In_{.53}Ga_{.47}As/In_{.52}Al_{.48}As$ ($\Delta E_c = 0.52$ eV and $\Delta E_v = 0.21$ eV) [73].

6.4. Conclusion

A new structure incorporating an $In_{.53}Ga_{.47}As/In_{.52}Al_{.48}As$ graded-superlattice grown by MBE to provide an enhanced effective Schottky barrier height on n-$In_{.53}Ga_{.47}As$ has been demonstrated for the first time. Excellent I-V and C-V characteristics and an overall effective Schottky barrier height of ~ 0.71 and ~ 0.60 eV for Au and Cr, respectively, have been achieved. This novel graded-superlattice Schottky barrier can be incorporated to high speed electronic and optoelectronic devices without any trapping effect of carriers at the high-low heterointerface.

CHAPTER SEVEN
PACKAGING OF A HIGH-SPEED PHOTODETECTOR

To deliver maximum power to a load without any significant attenuation and distortion of electrical and optical signals, impedance matching networks are necessary to properly terminate the input/output ports of device. However, the conventional packages are not suitable for a high-speed photodetector. Self-resonances, RF insertion loss, and impedance-mismatch are some of the problems encountered with the conventional packages. Furthermore, there exist another significant problems associated with high-frequency operation.

7.1. Microstrip Transmission Line

Transmission line structures which are commonly considered for microwave integrated circuits are illustrated in Table 7.1 along with their characteristic impedances, range of operating frequency, loss and dispersion, and integrability with various solid-state devices. Among them, the most frequently used transmission line is microstrip, mainly due to the fact that the mode of propagation on microstrip is almost transverse electro-magnetic (TEM). This allows an easy approximate analysis and yields wide band circuits.

Various methods of microstrip analysis may be divided into three groups. In the first group which comprises quasi-static method [74-77] the nature of propagation mode is considered to be pure TEM, and microstrip characteristics are calculated from the electrostatic capacitance of the structure. It is found that this analysis is adequate for designing circuits at lower frequencies (below X-band) where the strip width and the substrate thickness are much smaller than the wavelength in the dielectric material. In the second group, called dispersion models [78-81], the deviation from the TEM nature is accounted quasi-empirically.

Table 7.1 Various transmission line structures and characteristics.

Transmission line	Microstrip	Coplanar	Slot	Suspended
Structure				
Characteristic Impedance (Ω)	25-95	30-150	60-200	40-150
Frequency of Operation (GHz)	$\leq$ 100	$\leq$ 60	-	$\geq$ 100
Loss	Medium	High	High	Low
Dispersion	Low	High	-	High
Integrability (Series)	Easy	Easy	Difficult	Easy
Integrability (Parallel)	Difficult	Easy	Easy	Difficult

Some parameters of the model are determined such that the final expression agrees with the known experimental (or exact theoretical) dispersion behavior of the microstrip. The methods in the third group [82,83] take into account the hybrid nature of propagation mode.

7.1.1. Quasi-Static TEM Model

The microstrip synthesis problem consists of finding the values of width W and length ℓ corresponding to the characteristic impedance Z_o and electrical length θ defined at the network design stage. Initially a suitable substrate of thickness h and relative permittivity ϵ_r will have to be chosen. The synthesis actually yields the normalized width-to-height W/h initially, as well as a quantity called the effective microstrip permittivity ϵ_{eff}.

The general geometry of microstrip is shown in Fig.7.1. The most important dimensional parameters are the microstrip width W and height h. Also of main importance is the relative permittivity of the substrate ϵ_r. The thickness of the metallic top-conducting strip is generally of much lesser importance and may quite often be neglected.

For narrow strips with $Z_o > (44 - 2\epsilon_r)$ ohms,

$$\frac{W}{h} = \left(\frac{\exp H'}{8} - \frac{1}{4\exp H'}\right)^{-1} \tag{7.1}$$

where

$$H' = \frac{Z_o\sqrt{2(\epsilon_r + 1)}}{119.9} + \frac{1}{2}\left(\frac{\epsilon_r - 1}{\epsilon_r + 1}\right)\left(\ln\frac{\pi}{2} + \frac{1}{\epsilon_r}\ln\frac{4}{\pi}\right) \tag{7.2}$$

One may also use, with slight but significant shift of changeover value to $W/h < 1.3$ with $Z_o > (63 - 2\epsilon_r)$ ohms:

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2}\left[1 - \frac{1}{2H'}\left(\frac{\epsilon_r - 1}{\epsilon_r + 1}\right)\left(\ln\frac{\pi}{2} + \frac{1}{\epsilon_r}\ln\frac{4}{\pi}\right)\right]^{-2} \tag{7.3}$$

where H′ is given by Eq.(7.2) as a function of Z_o or, alternatively, as a function of W/h, from Eq.(7.1):

$$H' = \ln\left[4\frac{h}{W} + \sqrt{16\left(\frac{h}{W}\right)^2 + 2}\right] \tag{7.4}$$

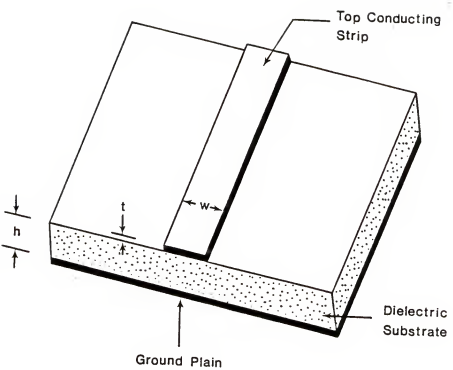


Figure 7.1 General geometry of a microstrip line.

For wide strip with $Z_o < (44 - 2\epsilon_r)$ ohms,

$$\frac{W}{h} = \frac{2}{\pi}[(d_e - 1) - \ln(2d_e - 1)] + \frac{\epsilon_r - 1}{\pi\epsilon_r}\left[\ln(d_e - 1) + 0.293 - \frac{0.517}{\epsilon_r}\right] \tag{7.5}$$

where

$$d_e = \frac{59.95\pi^2}{Z_o\sqrt{\epsilon_r}} \tag{7.6}$$

With the same slight shift of changeover value as before where $W/h > 1.3$ and $Z_o > (63-2\epsilon_r)$ ohms, a modified form of effective permittivity is given by

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left(1 + 10\frac{h}{W}\right)^{-0.555} \tag{7.7}$$

Alternatively, provided Z_o is known first, then

$$\epsilon_{eff} = \frac{\epsilon_r}{0.96 + \epsilon_r(0.109 - 0.004\epsilon_r)[\log(10 + Z_o) - 1]} \tag{7.8}$$

In Fig.7.2, shape ratio (W/h) versus characteristic impedance (Z_o) is shown for the various substrate materials without considering the effects of top conducting strip thickness (t).

For microstrip having $t/h \leq 0.005$, $2 \leq \epsilon_r \leq 10$, and $W/h \geq 0.1$, the effects of this thickness are negligible. Whereas, at smaller values of W/h or greater values of t/h, the significance increases. Then, the effective microstrip permittivity ϵ_{eff} can be expressed by

$$\epsilon_{eff}(t) = \epsilon_{eff} - \Delta\epsilon_{eff}(t) \tag{7.9}$$

where

$$\Delta\epsilon_{eff}(t) = \frac{(\epsilon_r - 1)t/h}{4.6\sqrt{W/h}} \tag{7.10}$$

7.1.2. Dispersion Model

There are nonlinear characteristics between the frequency of signal (above a few GHz) exciting a microstrip line and the phase constant or wave number $\beta(= 2\pi/\lambda_g)$, due to the hybrid mode of propagation along the microstrip line. All microstrip line structures exhibit this type of behavior, so called, dispersion. Most of the closed-formula expressions for

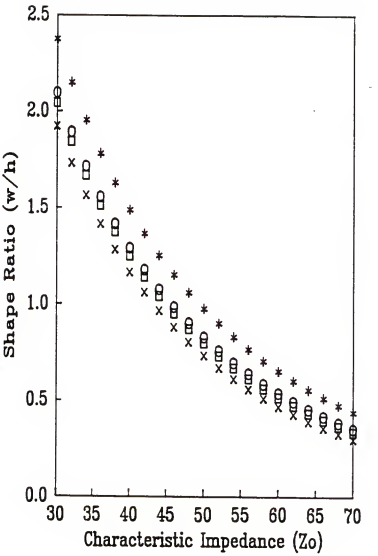


Figure 7.2 Shape ratio (W/h) versus characteristic impedance (Z_o) for the various substrate materials without considering the effects of top conducting strip thickness. (*:alumina, o:sapphire, □:silicon, ×:gallium-arsenide)

calculating dispersion require the static-TEM values of ϵ_{eff}, and sometimes Z_o as well. These values may be obtained by the methods given in previous section. Thus, the frequency-dependent effective microstrip permittivity [78] can be written as a function involving ϵ_{eff} and Z_o as follows:

$$\epsilon_{eff}(f, \epsilon_{eff}, Z_o) = \epsilon_r - \frac{\epsilon_r - \epsilon_{eff}}{1 + (\pi^2/12)A^2B} \tag{7.11}$$

$$A = \left(\frac{2f\mu_o h}{Z_o}\right) \tag{7.12}$$

$$B = \left[\frac{(\epsilon_{eff} - 1) + (h'/h)^2(\epsilon_r - \epsilon_{eff})}{\epsilon_r - 1}\right]\left[\frac{(\epsilon_{eff} - 1)(\epsilon_r - \epsilon_{eff})}{\epsilon_{eff}(\epsilon_r - 1)}\right] \tag{7.13}$$

There is only one unknown parameter in this expression, and that is h'/h. It turns out that this parameter varies little as a function of Z_o over quite a wide range. In Fig.7.3, frequency-dependent effective permittivity ($\epsilon_{eff}(f)$) is shown as a function of frequency by considering the effects of top conducting strip thickness.

Formula for the frequency-dependent characteristic impedance given by Bianco et al.[80] is

$$Z_o(f) = Z_{oT} - \frac{Z_{oT} - Z_o}{1 + G(f/f_p)^2} \tag{7.14}$$

where

$$f_p = \frac{Z_o}{2\mu_o h} \tag{7.15}$$

$$G = \left(\frac{Z_o - 3}{60}\right)^{1/2} + 0.001Z_o \tag{7.16}$$

and μ_o is the free-space permeability ($4\pi \times 10^{-7}$ H/m). The parameter G is purely empirical, thereby giving some flexibility to the formula. G is dependent mainly on Z_o but also, to a lesser extent, on h.

The design algorithms for the microstrip width with a given frequency-dependent characteristic impedance are

1. As an initial approximation, let $Z_o(f) \simeq Z_o$.

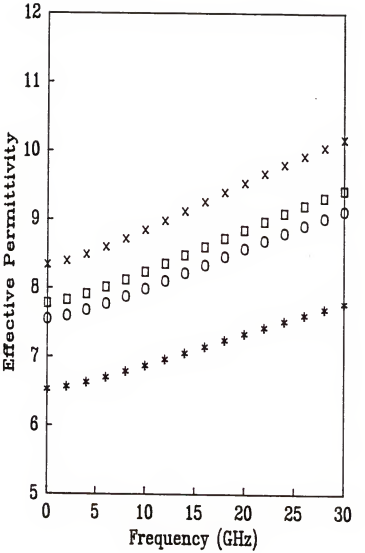


Figure 7.3 Frequency-dependent effective permittivity $\epsilon_{eff}(f)$ versus frequency by considering the effects of top conducting strip thickness. (∗:alumina, ○:sapphire, □:silicon, ×:gallium-arsenide)

2. Find the approximate microstrip width W with ϵ_r and h.

3. Determine the frequency-dependent denominator $\{1 + G(f/f_p)^2\}$, of Eq.(7.14) using this approximate value of Z_o.

4. Evaluate Z_{oT} for triplate having the same strip width W as the microstrip, but twice the dielectric thickness (2h). Design curves or good approximations may be used.

5. Rearrange Eq.(7.14) for Z_o, letting $A = \{1+G(f/f_p)^2\}$. This is $Z_o = A\{Z_o(f) - Z_{oT}\} + Z_{oT}$.

6. With this approximate value of Z_o, calculate W/h using static-TEM expressions, and hence calculate W.

7. Repeat steps (2)-(6) until negligible difference is observed in the values of w obtained (e.g., it may be desired that the result should be accurate to within 1 %).

7.1.3. Q-Factor and Power Loss

Four separate mechanisms can be identified for power losses and parasitic effects associated with microstrip lines; (1) conductor losses, (2) dissipation in the dielectric of the substrate, (3) radiation losses, and (4) surface-wave propagation. The first two items are dissipative effects, whereas radiation loss and surface-wave propagation are essentially parasitic phenomena. Considering a fictitious microstrip resonator, which does not radiate or propagate surface-waves, the dissipative losses may be interpreted in terms of a Q-factor defined as

$$Q = \frac{\omega_o U}{W} \tag{7.17}$$

where U is the stored energy and W is the average power lost per cycle. With V_p and I_p, the peak voltage and current at some plane along the line, Eq.(7.17) becomes

$$Q = \omega_o \frac{(LI_p^2/2 + CV_p^2/2)/2}{(RI_p^2 + GV_p^2)/2} \tag{7.18}$$

With the relations of $I_p = V_p/Z_o$, $Z_o = \sqrt{L/C}$, $\beta = \omega\sqrt{L/C}$, and $\alpha = R\sqrt{C/L} = R/Z_o$, Eq.(7.18) can be rearranged as

$$Q = \frac{\beta}{2\alpha} \tag{7.19}$$

The phase coefficient β is identical to $2\pi/\lambda_g$, then Eq.(7.19) finally becomes

$$Q = \frac{\pi}{\alpha\lambda_g} \tag{7.20}$$

The conductor loss can be given by [81]

$$\alpha_c = 0.072\frac{\sqrt{f}}{WZ_o}\lambda_g \tag{7.21}$$

where f is in gigahertz and Z_o is in ohms. An improved formula considered the surface roughness effect is given by

$$\alpha_c' = \alpha_c\left[1 + \frac{2}{\pi}\arctan\left\{1.4\left(\frac{\Delta}{\delta_s}\right)^2\right\}\right] \tag{7.22}$$

where Δ is the rms surface roughness; $\delta_s = 1/(R_s\sigma)$ is the skin depth at the operating frequency; R_s is surface resistance; σ is metal film conductivity.

The dielectric loss has been analyzed by several workers. Gupta et al. [77] derived the following expression for dielectric attenuation coefficient, α_d, per unit length:

$$\alpha_d = 27.3\frac{\epsilon_r(\epsilon_{eff} - 1)\tan\delta}{\sqrt{\epsilon_{eff}}(\epsilon_r - 1)\lambda_o} \tag{7.23}$$

where $\tan\delta$ is the loss tangent for the substrate material.

7.2. Planar Lumped Elements

Recent developments in microwave integrated circuits have extended the use of planar lumped elements [84-88], such as planar capacitors, planar inductors, and planar resistors, particularly for broadband circuits with minimal size requirements. However, it is difficult to realize a true lumped element, even at the lower microwave frequencies, because of the parasitics to ground that are associated with the thin substrate. In the following subsections, the design principles of planar lumped elements will be described.

7.2.1. Planar Capacitor

There are basically two types of planar capacitors suitable for microwave band: One is the overlay structure employing dielectric films, and are suitable for low-impedance circuitry of bypassing and blocking applications. The other does not use a dielectric film but depends on electrostatic coupling via the substrate. These are generally suitable for applications where low values of capacitance (< 1.0 pF) are required for high-impedance matching circuits.

A perspective view of an overlay thin-film capacitor and its equivalent circuit are shown in Fig.7.4. Taking into account the longitudinal current paths in the metal contacts, one can analyze this structure as a lossy transmission line. L and r represent the inductance and resistance per unit length of the metal plate, and c and g denote the capacitance and conductance per unit length of the dielectric film. The relation between g and c is determined by the loss tangent, $g = \omega c \tan \delta_d$. The series resistance in the plates is governed by the skin resistance if the metal thickness exceeds the skin depth, or by the bulk resistance for the reverse condition. From the equivalent circuit model, the impedance of the thin-film capacitor can be expressed as

$$Z(\omega) = \frac{Z}{\gamma}\left[\cosh\left(\frac{\gamma\ell}{2}\right) + \frac{\gamma\ell}{2}\right] \tag{7.24}$$

where

$$\gamma = \sqrt{2(g + j\omega c)(r + j\omega L)} \tag{7.25}$$

and

$$Z = r + j\omega L \tag{7.26}$$

For well-designed capacitor, where the capacitor length is small compared to the wavelength in the dielectric film, $|\gamma\ell| \ll 1$. Then, the frequency dependent impedance of a thin-film capacitor becomes

$$Z(\omega) \approx \frac{1}{j\omega C} + j\frac{2}{3}\omega L\ell + \frac{2}{3}r\ell + \frac{\tan \delta_d}{\omega C} \tag{7.27}$$

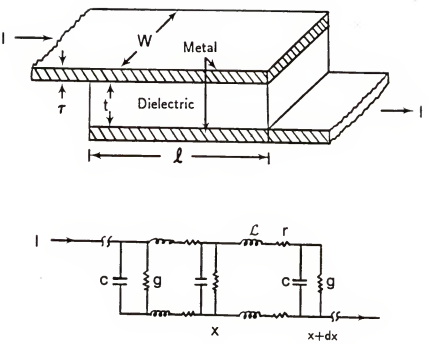


Figure 7.4 Schematic diagram and its equivalent circuit model for the analysis of the impedance of a thin-film capacitor.

where $C = c\ell$ is the total capacitance. Note that the total resistance $2r\ell/3$ is equal to $2R/3$, where R is the sum of the resistance of the top and bottom plates. The 1/3-factor is introduced because the current distribution along the length of the electrodes is not uniform but linearly dependent to the distance.

If one assumes that the losses in the electrodes are predominatly skin losses (not necessary true for the bottom electrode), the Q-factor corresponding to conductor losses is given by

$$Q_c = \frac{3}{2\omega R_s(C/A)\ell^2} \tag{7.28}$$

where R_s is the surface skin resistivity. If both electrodes are several skin-depths thick, then Q_c decreases with the 3/2 power of frequency. However, in practice, the bottom plate is less than a skin-depth thick, and its resistance predominates. In this case, R_s reverts to the bulk resistance (frequency-independent) and Q_c decreases inversely with frequency. The total Q-factor is given by

$$\frac{1}{Q} = \frac{1}{Q_c} + \frac{1}{Q_d} \tag{7.29}$$

where $Q_d = \cot \delta_d$ is the dielectric Q-factor.

7.2.2. Planar Inductor

Planar inductors can be realized in a number of configurations, all achieved with a single- or double-layer metallization scheme. Aside from the high-impedance line section, all of the structures depend on mutual coupling between the various line segments to achieve high inductance in a small area. In any multisegment design, one must ensure that the total line length ia a small fraction of a wavelength.

A simple but reliable calculation for the inductance of a rectangular can be made by a summation of all the self- and mutual-inductances of the various finite line segments comprising the inductor, provided that there is no phase shift in the current from element to element. The inductance of a high-impedance line section, on the other hand, can be

given by

$$L = \frac{Z_o}{v}\ell \tag{7.30}$$

which is the product of the line length and the ratio of the characteristic impedance and the phase velocity.

To calculate the more accurate inductance of planar inductors, corrections must be made for the image inductance induced by the conducting ground plane. The effect of the ground plane is to decrease the inductance with the amount of reduction which is inversely proportional to the substrate thickness. It can be shown that the amount of reduction is simply equal to the mutual inductance, M, between the given planar inductor and its mirror image below the ground plane. Thus, if L_o is the self-inductance of the planar inductor, and M(s) is the mutual inductance between it and its image separated by a distance s, the net inductance of the planar inductor is given by

$$L = L - M(2h) \tag{7.31}$$

where h is the substrate thickness. The total inductance and the image inductance for a square spiral inductor is shown in Fig.7.5, as a function of the number of line segments (4 segment = 1 turn), starting from the outermost segment and proceeding inward. Typical inductance values for monolithic circuits fall in the range from 0.5 to 10 nH.

The quality factor of spiral inductors is not very high, especially in the lower microwave band. The predominant source of loss is the ohmic resistance of the conductors. Somewhat higher Q-factors are achievable with microstrip resonant stub sections. These are more properly considered as distributed resonant elements. Assuming negligible dielectric loss, one may show that the conductor Q-factor for a quarter-wave open circuit stub is given by

$$Q_c = \frac{27.3}{\alpha\lambda_g} \tag{7.32}$$

where $\alpha\lambda_g$ is the loss in the line section in dB/wavelength. Since $\alpha\lambda_g$ decreases as $f^{-1/2}$,

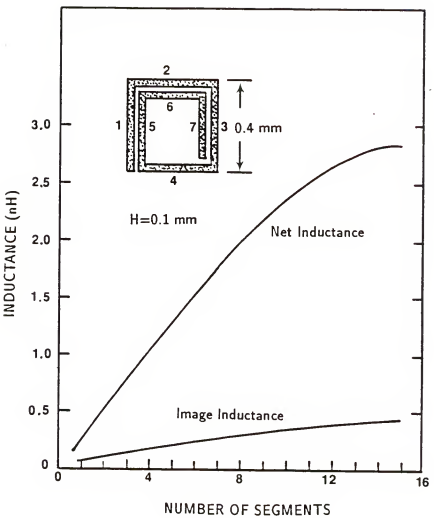


Figure 7.5 Inductance of a rectangular spiral on a GaAs substrate as a function of the number of segments. (line width=0.025 mm and line separation=0.025 mm)

Q_c increases as the square root of frequency. On the other hand, radiation losses vary as

$$Q_r = \frac{R}{(fh)^2} \tag{7.33}$$

where h is the substrate thickness and R is a function of W/h and the dielectric constant of the substrate. (The radiation factor R is considerably large for a quarter-wave stub grounded at its far end.) It should be noted that any attempt to increase the conductor Q-factor by increasing the frequency and substrate thickness is eventually overcompensated by the decrease in radiation Q-factor.

7.2.3. Planar Resistor

Planar resistors are used for a variety of purposes, such as loads for FETs, terminations for couplers and power combinders, as damping resistors to equalize the gain over a wide bandwidth, as stabilizing resistors to prevent parasitic oscillations, and as voltage dividers and dropping resistors in dc supply lines. Some factors to be considered in the design of planar resistors are (1) the sheet resistivity available, (2) the thermal stability and temperature coeeficient of the film, (3) the frequency bandwidth of the resistor, and (4) the thermal resistance.

Planar resistors can be fabricated in various forms which all fall into one of three categories; (1) semiconductor films, (2) deposited metal films, and (3) ceramic metals (cermets). Resistors based on semiconductors can be fabricated by forming isolated land of conducting semiconductor film on the substrate. Metal-film resistors are formed by the evaporation of a metal layer over the substrate and by the definition of the desired pattern. Cermet resistors are fabricated by films consisting of a mixture of metal and a dielectric.

A problem common to all planar resistors used at high frequencies is the parasitic capacitance to the ground plane. The distributed shunt capacitance (and series inductance) introduces a frequency dependence to the resistor. This frequency dependence can be detemined by treating the resistor as a very lossy microstrip line, as is shown in Fig.7.6. A

strightforward analysis leads to the following expression for the impedance of the resistor

$$Z(\omega) = R_{dc}\left[AB \tanh\left(\frac{A}{B}\right)\right] \tag{7.34}$$

where R_{dc} is the dc resistance of the film, and

$$A = \sqrt{1 + j\frac{Z_o}{R_{dc}}\Theta} \tag{7.35}$$

$$B = \sqrt{\frac{Z_o}{R_{dc}}\frac{1}{j\Theta}} \tag{7.36}$$

$$\Theta = \frac{\omega \ell}{v} \tag{7.37}$$

Here, Z_o and v are the characteristic impedance and phase velocity of the resistive segment treated as a lossless trnsmission line. Both Z_o and v are functions of W/h and dielectric constant of the substrate. For low thermal resistance, the area of the film must be as large as possible, and discontinuity effects in width must be minimized. This means that the resistive element should be as long as possible to minimize thermal resistance. This length is specified by the sheet resistivity of the film which is given by

$$\ell = \frac{WR_{dc}}{\rho_s} \tag{7.38}$$

where W is the width of the film.

7.2.4. Junction and Discontinuity

In the design of microstrip transmission line, there are many junctions and discontinuities which introduce unwanted parasitic inductances and capacitances. Figure 7.7 illustrates the circuit representations of the junctions and discontinuities in microstrip line. Since such dicontinuities cannot be avoided, their frequency dependancies must be taken into account, especially for operation above the X-band. It should be noted that a frequency dependance is intrinsic to each discontinuity. The behavior of these junctions is even more complex than may be inferred from the simplicity of the equivalent circuits because these circuits are valid over a restricted frequency band. For a broad band frequency range, the

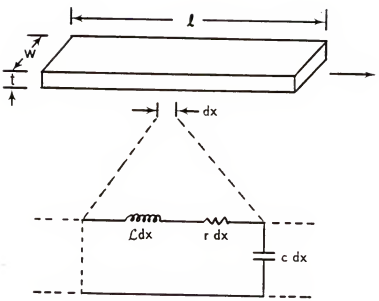


Figure 7.6 Model for the differential element of a thin-film resistor.

properties of the junctions should be characterized in terms of scattering parameters for a given frequency band. It is important to include the junction effects in a broad band circuit design. The circuit layout cannot be exactly predicted in advance. The junction effects, therefore, must be added into the design after the initial mask layout. A second optimization of the circuit can be made at this step to allow readjustment of circuit element values.

7.3. Impedance Matching Networks of A High-Speed Photodetector

The design procedures for the impedance matching networks of a high-speed photodetector consist of graphical approximations, computer aided circuit synthesis and optimization, and evaluation, and are shown in Fig.7.8. Impedance matching circuits for a high-speed photodetector can be easily designed using the normalized impedance and admittance (ZY) Smith chart, which is basically a plot of all passive impedances in a relfection coefficient chart of unit radius. The Smith chart is also used to present the frequency dependence of scattering parameters and other device characteristics.

Designing an impedance matching networks in the ZY Smith chart consists of moving along a constant-resistance or constant-conductance circle from one value of impedance or admittance to another. Each motion along these constant circles corresponds to the appropriate element of the matching networks. The four types of motions are shown in Fig.7.9. The effect of adding a series inductor (capacitor) is to move in a clockwise (counterclockwise) direction along a constant-resistance circle. On the other hand, the effect of adding a shunt inductor (capacitor) is to move in a counterclockwise (clockwise) direction along a constant-conductance circle.

The detailed procedures for the optimum packaging of a high-speed photodetector are as follow:

1. Establish the desired specification.

   Matching networks for a photodetector should be impedance-matched to a 50 Ω exter-

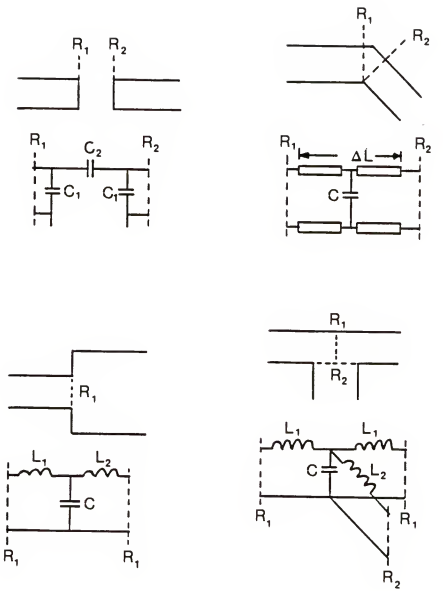


Figure 7.7 Circuit representations of the junctions and discontinuities in microstrip transmission line.

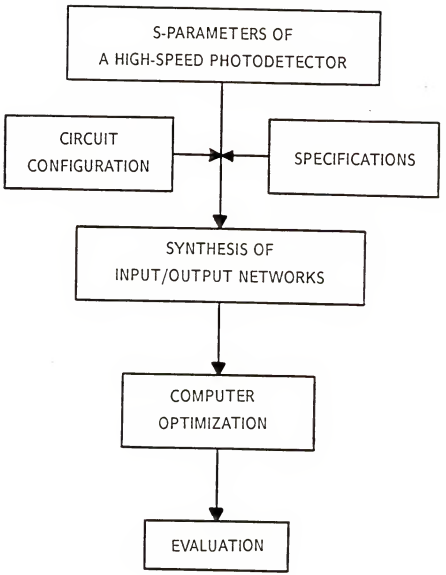


Figure 7.8 Design procedures for the optimum packaging of a high-speed photodetector.

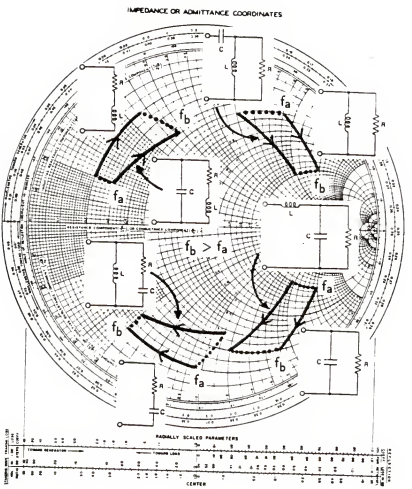


Figure 7.9 Effects of adding series and shunt elements in the impedance-admittance (ZY) Smith chart.

nal load with minimum parasitics. In addition, packaging should have large dynamic range and broadband operation.

2. Obtain the S-parameter of the photodetector.

   The scattering parameter (S_{11}:reflection coefficient) of a photodetector can be measured by using HP 8510A Network Analyzer for microwave frequencies ($1 \sim 20$ GHz). The measured reflection coefficients of the planar GaAs Schottky barrier photodiode is shown in Fig.7.10. The inductance of the bonding wire is assumed to be 20 nH/inch. It should be noted that the reflection coefficients of the photodetectors differ from device to device. Hence, it is difficult to say that matching networks designed for one photodetector should be used for the other photodetector.

3. Model the photodetector with distributed elements.

   In order to synthesize the matching networks, the input impedance of a photodetector must be described by the separated resistive and reactive components. The resistive part of the device model can be directly read off the constant-resistance and constant-reactance circles of the Smith chart. The synthesis is, then, carried out between the resistive terminations, and the reactive parts will be absorbed in the matching networks.

4. Synthesize the input/output networks.

   All network elements can be realized in microstrip form, except the series open stub that is to be fully absorbed as the reactive part of the photodetector input. At the necessary minimum insertion loss, the matching networks will be synthesized and scaled to 50 Ω. If the characteristic impedances of the input/output are too high for the conventional microstrip line, the impedances could be adjusted by network transformations.

5. Optimize the complete matching networks.

   The choice of the network configurations is typically based on the simplification of the topology to be designed. The optimization can be done via the general-purpose computer programs such as COMAC (Computerized Optimization of Microwave Amplifier Circuits) and CADSYN.

6. Evaluate the circuits.

   The final evaluation of the matching networks should be performed to meet the initially designed specifications.

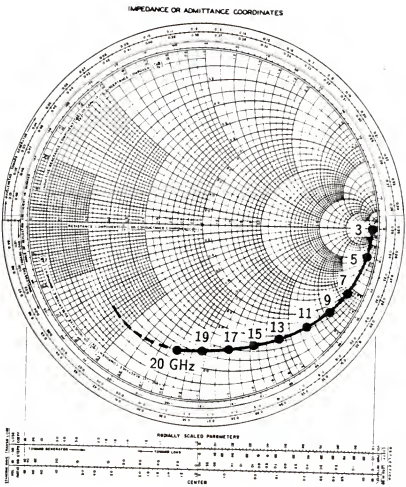


Figure 7.10 Measured S-parameter (S_{11}:reflection coefficient) of a planar GaAs Schottky barrier photodiode.

CHAPTER EIGHT
SUMMARY, CONCLUSIONS, AND RECOMMENDATIONS

8.1. Summary and Conclusions

The main objectives of this dissertation are the development of high-speed photodetectors (up to 50 GHz) and the optimum package for optical computing and communications. For the low-noise high-speed photodetectors, n-type GaAs and p-type $In_{.53}Ga_{.47}As$ planar Schottky barrier photodiodes have been designed, fabricated, and characterized. In order to minimize the packaging parasitics of a high-speed photodetector, which may attenuate or distort both electrical and optical signals if not properly designed, impedance matching networks for a high-speed photodetector have been developed by employing microstrip transmission line or coplanar waveguide. The main results are summarized as follows:

1. A systematic study of surface passivations and antireflection coatings for GaAs and $In_{.53}Ga_{.47}As$ photodiodes has been carried out using various dielectric films such as SiO_2, Si_3N_4, and polyimide. The results have shown that Si_3N_4 on GaAs and polyimide on $In_{.53}Ga_{.47}As$ are the most effective dielectric films for reducing the leakage current and reflection loss.

2. For the detection of short wavelength optical signals, a high-speed, high-sensitivity planar $GaAs/Al_{0.3}Ga_{0.7}As$ heterostructure Schottky barrier photodiode has been designed, fabricated, and characterized. A highly doped n^+-$Al_{0.3}Ga_{0.7}As$ buffer layer has been used to reduce the series resistance and the undesired diffusion tailing. Furthermore, surface passivation and antireflection coating with Si_3N_4 film have been performed to reduce the reverse-bias dark current and the reflection loss of the incident light, which significantly improve the sensitivity of a photodiode. The measured

external quantum efficiency and responsivity are 60 $\sim$ 77 % and 0.47 $\sim$ 0.6 A/W, respectively, for the wavelength range of 0.5 $\sim$ 0.84 μm. A risetime of 8.5 ps and a 3-dB cutoff frequency of 50 GHz have been determined from the sampling/correlation measurements.

3. For long wavelength use, a high-speed planar back-to-back Schottky barrier photodiode on p-$In_{.53}Ga_{.47}As$/p^+-InP/semi-insulating InP substrate has been designed, fabricated, and characterized. The measured external quantum efficiency and responsivity of the polyimide coated photodiode are 48 $\sim$ 69 % and 0.49 $\sim$ 0.56 A/W, respectively, for the wavelength range of 0.9 $\sim$ 1.8 μm. The computer simulation (e.g., SLICE) for the equivalent circuit model of the photodiode has shown that the 3-dB cutoff frequency is 2.7 GHz.

4. A new structure to enhance the effective Schottky barrier height on n-$In_{.53}Ga_{.47}As$ has been demonstrated for the first time by using a novel $In_{.53}Ga_{.47}As/In_{.52}Al_{.48}As$ graded-superlattice grown by MBE. Excellent I-V and C-V characteristics and an overall effective Schottky barrier height of $\sim$ 0.71 and $\sim$ 0.60 eV for Au and Cr, respectively, have been achieved. This new graded-superlattice Schottky barrier can be incorporated to high speed electronic and optoelectronic devices without any trapping effect of carriers at the high-low heterointerface.

5. To deliver the maximum power of a high-speed photodetector to the external load without any significant attenuation and distortion, impedance matching networks with minimum parasitics have been developed.

   (a) Characteristics of the microstrip transmission line parameters such as impedance, attenuation factors, and dispersion relation have been analyzed, and the design algorithm for microstrip line has been established.

   (b) Design principles of the planar lumped elements such as inductor, capacitor, re-

sistor, and junction discontinuity have been discussed based on the characteristic impedances and the quality factors.

(c) Design procedures for the impedance matching networks consisted of graphical approximation, computer aided circuit synthesis and optimization, and evaluation have been developed.

8.2. Recommendations for Further Study

Monolithically integrated optical receiver module, which consists of a high-speed photodetector, a low-noise transimpedance amplifier, and lumped and distributed passive elements, can provides the improved performance and reliability, the increased functionality, the economy of size and scale, and the resulting proliferation of the computer industry. For high-speed photodetectors, a planar interdigitated metal-semiconductor-metal (IMSM) Schottky barrier photodiode and its 2-dimensional detector array are the most suitable candidates due to the simplicity of fabrication and integration. For the amplifier unit, low-noise FETs such as enhanced/depleted MESFETs with a common source configuration should be used to obtain a good voltage gain and a low noise figure. If a good input match is necessary along with a low noise figure, either a balanced amplifier or a common gate input circuit can be used.

The optimally designed detector/amplifier circuitry via computer aided design (CAD) should be fabricated on the semi-insulating substrates with thin film components such as planar inductor, resistor, capacitor, and transmission line. To achieve minimum parasitics and maximum performance of the monolithically integrated photoreceiver module, the requirements for the interconnections and packages are low insertion loss, wide bandwidth, reproducibility, RF match, and small size. Characterizations of the photoreceiver module can be performed on the test fixture which has a 50 ohm input/output impedance.

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BIOGRAPHICAL SKETCH

Doo-Hwan Lee was born in Seoul, Republic of Korea, on October 7, 1957. He completed the degree of Bachelor of Engineering in the electronics engineering from the Yonsei University in 1980. From 1980 to 1982, he worked with the Communication Division of R.O.K. Army where he was engaged in the design of noiseless pulse coded modulation system as a first lieutenant. He received the degree of Master of Engineering in electrical engineering in 1986 from the University of Florida. Since May 1986, he has been working toward the degree of Doctor of Philosophy at the University of Florida.

His present interests include the development of III-V compound semiconductor high speed photodetectors and two-dimensional detector array, and high power lasers utilizing superlattice and quantum well structures.

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Sheng S. Li, Chairman
Professor of Electrical Engineering

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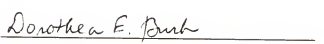

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I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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This dissertation was submitted to the Graduate Faculty of the College of Engineering and to the Graduate School and was accepted as partial fulfillment of the requirements for the degree of Doctor of Philosophy.

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